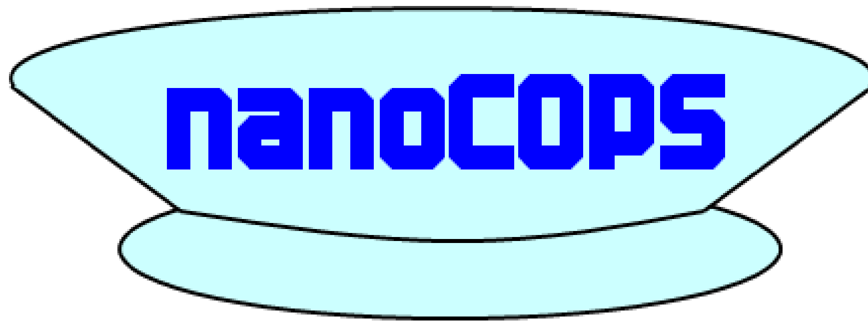

Project:	**nanoCOPS**
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Tasks:	T3.2 Specification of tests for final validation (test plan) T3.3 Measurements
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Title:	**Specification of Validation tests (test plan) and Measurement setup**
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Affiliation(s):	NXP, BUW, ACC, FHO, MPG, BUT, MAG, ONN, UGW, TUD
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1 Introduction

One of the objectives of Work package WP3 is to facilitate validation of new algorithms/tools and modelling methodologies developed during the project, by:

- Comparison with available designs and experimental results. An inventory will be made to set up a number of relevant test cases from the repositories of the end-user partners.
- Comparison with simulation results of the tools/algorithms developed within the project against the results obtained with the existing commercial and/or public domain tools.

Related to this, in the first phase of the project, work was performed in Task T3.1, "Tool development test set and data format specification", which dealt with test cases and with a test set.

T3.1 (part a) Tool development test set
An inventory will be made of available (circuit) test cases, preferably with existing experimental results at the end-user sites, and a test cases repository will be formed. The sample cases from the repository should cover all possible types of structures that are suffering from targeted problems to be solved in this project, to be used as working material for WP1-WP2, but also for final validation. The purpose is to simulate the test cases (including the two Use Cases) with the tools which have been developed in WP1-WP2.

The first deliverable D3.1 (part a): "Tool Development Test Set" was the outcome of this specific task in WP3. It gives a description of a number of selected test cases from the industrial partners in the project.

A comprehensive validation of developed algorithms/tools will be done later using the test cases from the development test set. During this phase feedback will be given, such that some final fine-tuning can be done on the prototype toolset, if necessary. After the development phase, at the end of the project, a final validation of the algorithms, using a few larger/more complex test cases, will be done.

The current deliverable D3.2 "Specification of Validation Tests (test plan) and Measurement setup" is the outcome of Tasks T3.2 and T3.3 (phases 1 and 2): "Specification of tests for final validation (test plan)" and "Measurements". These tasks started at T0+7 and T0, respectively, and the specific task descriptions are given as follows:

T3.2 A test plan will be developed for validation on the tool development test set of all prototype algorithms to be developed in WP1-WP2. The specification of the tests analysis will be defined in this phase. The specification will be addressed in terms of voltage, current, temperature and time range from one side, and in

terms of computation/simulation time and memory occupation on the other side. An algorithm of automated tests that covers all the specifications mentioned above will be developed.
The first activity will be to choose a representative minimal subset of benchmark structures to do the validation. The test plan described in this document will be based on this subset. However, should time permit, then it is always interesting to perform more tests.
In general, the test cases are quite relevant for the development work packages WP1-WP2, since they require a very strong cooperation between the results of the different work packages, making it impossible to simulate when this is not optimally achieved.

T3.3 (phases 1 and 2) In this task, the methodologies, test beds and procedures for RF measurements, as well as for possible EMC and ESD testing, and for heat and stress measurements will be prepared to meet the measurement requests of industrial and academic partners of the project. The task will be solved in four phases, of which the first 2 phases are related to the measurement setup:

- Phase one will take the first nine months of the project solution and deals with the measurement methodologies and scenario definitions. These will be designed based on partners' requests and inputs regarding expected results within the final stage of the project.
- Phase two will be realized during the next nine months and in this period the test bed setup and initial measurements will be realized based on current chip solutions of end-user partners.

2 Validation using available test cases (with ref. to deliverable D3.1a)

The purpose of using test cases is the validation of the simulation tools, in the use mode. The focus is on comparing the results of measurements and simulation for real-life size applications.

2.1 *Test case 1 – A realistic-size power MOS at constant temperature*

Test case 1 deals with a design provided by ON Semiconductor. We consider here operation at constant temperature and the focus is on computing Rdson. The structure consists of 4 layers.

The layout of the structure is shown in the next 6 plots. In Fig. 2.1 we see the top metal. In Fig. 2.2 we find the contact layer. Two zoom-ins are found in Fig. 2.3 and Fig. 2.4. We continue with zoomed plots of the 3rd and fourth layer in Fig, 2.5 and Fig. 2.6.

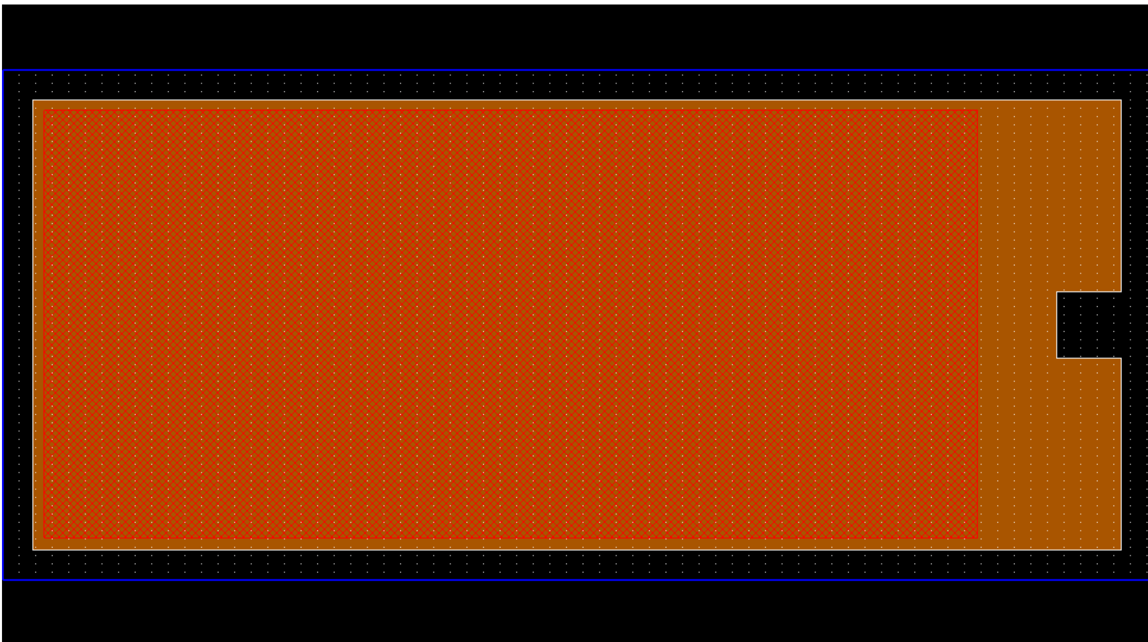


Fig. 2.1: Top metal

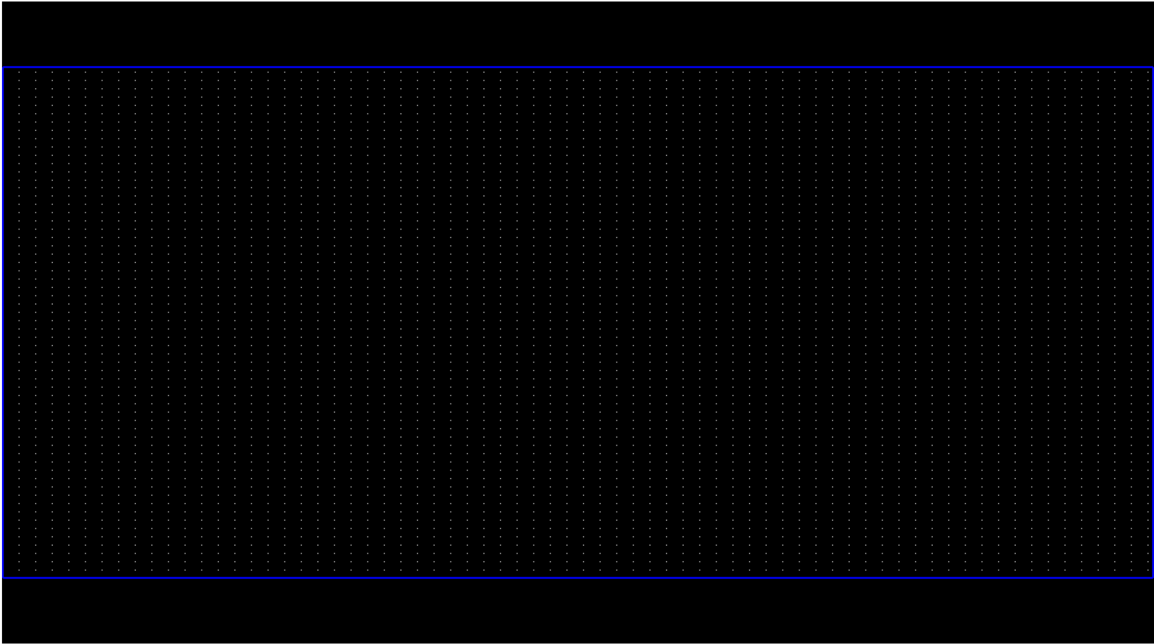


Fig. 2.2: Global view of the contact layer

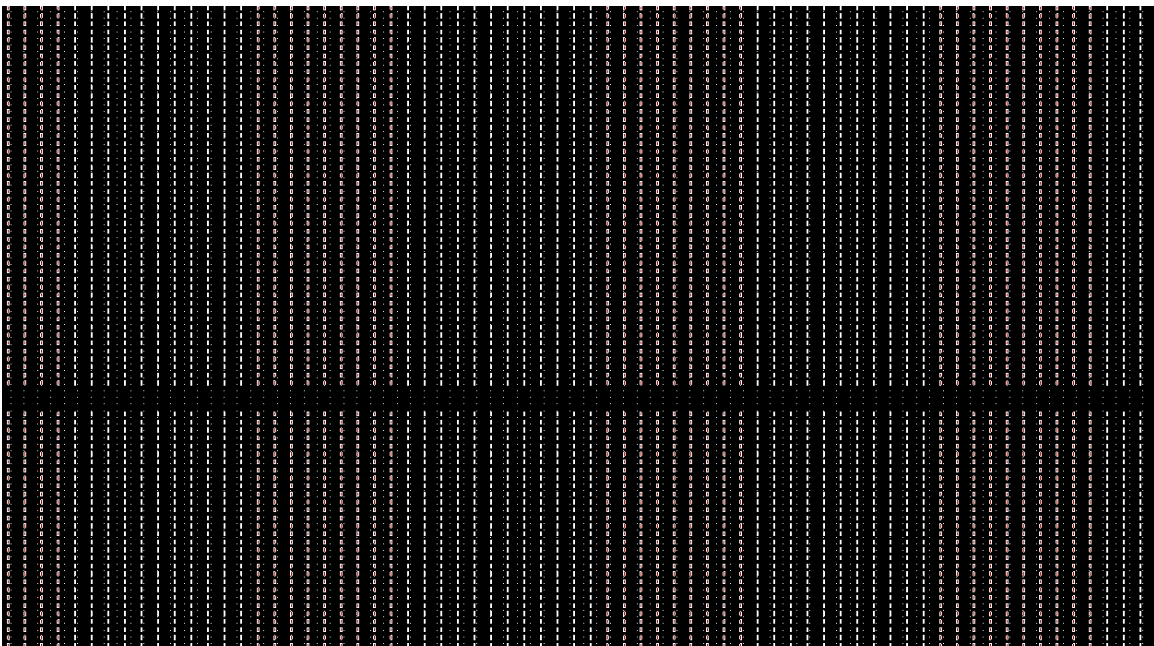


Fig. 2.3: Zoom-in view of the contact layer

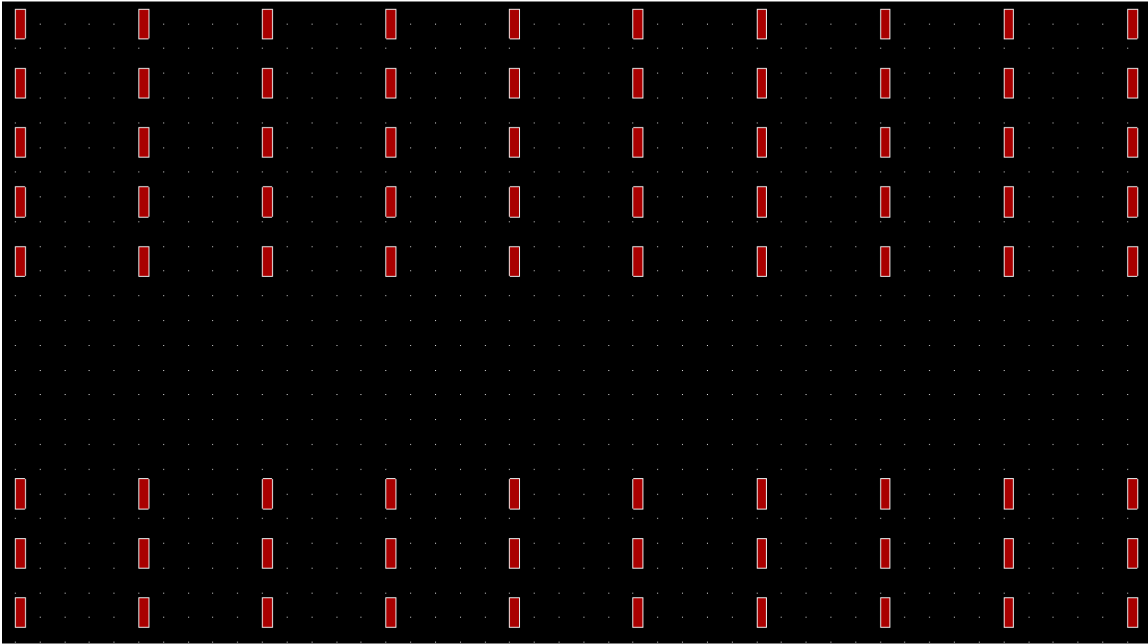


Fig. 2.4: Detailed zoom-in view of the contact layer. The horizontal separation between the vias is 5 micron. The vertical separation is 1 micron.

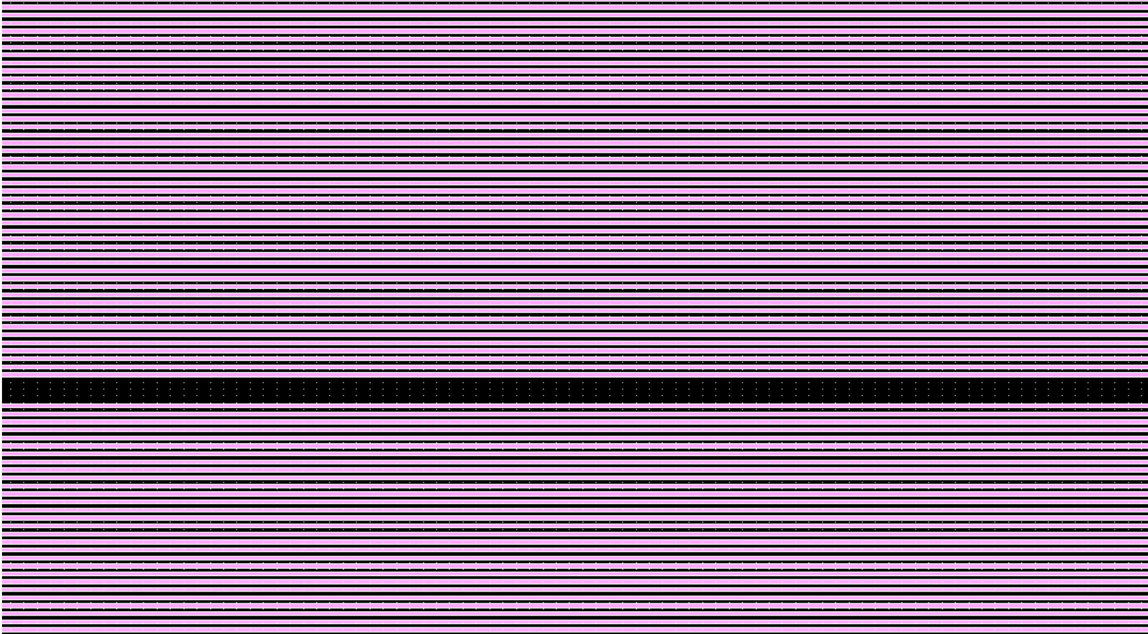


Fig. 2.5: Zoom in view of the channel layer

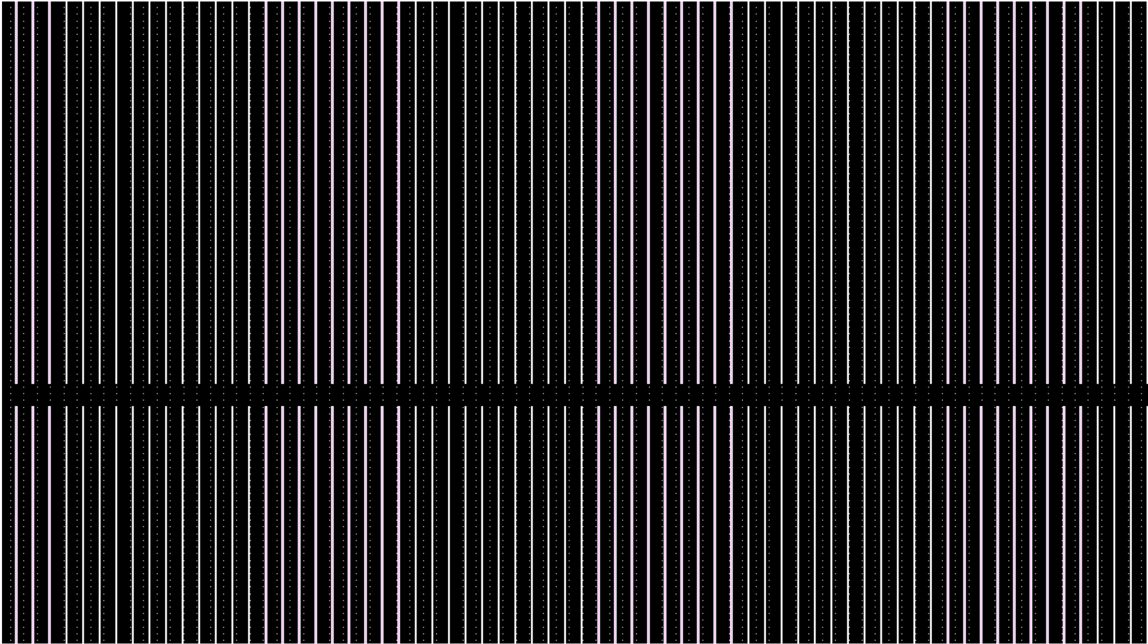


Fig. 2.6: Zoom in view of the active layer.

When launching the PTM (Magwel's Power Transistor Modeler) solver, the required mesh consists of 19012508 nodes.

The test is done for an applied voltage difference VDS=0.1V
The test should produce the following results

The total resistance:

- R_total
- P_total

R_metal breakdown:

- R_Drain_metal
- Power_Drain_metal
- R_Active
- Power_Active
- Power_Channel
- R_Contact
- Power_Contact
- R_Metal2
- Power_Metal2

2.2 *Test case 2 – A realistic-size power MOS in ET coupling mode*

The next test case represents a realistic industrial power MOS device from ON Semiconductor. Measurement data are available and the full strength of the ET (Electro-thermal) solver is addressed by both computation speed and memory footprint. Another interesting aspect of this test case is that the impact of packaging and the substrate is also accounted for. Therefore, being successful on this test case means that one project goal, e.g., the construction of an electro-thermal solver, both in the strong coupling mode as well as the co-simulation mode, is achieved. The material of the metals and vias is Aluminum. The material of the contacts is Tungsten, which has 174 W/Km as thermal conductivity, and 2.55E+6 J/Km^3 as heat capacity per unit volume. The limiting factor in this test case is the dynamic response, e.g., the static solution is aimed for. A full dynamic response is described in the next section.

The floorplan of the full test chip is shown in Fig. 2.7

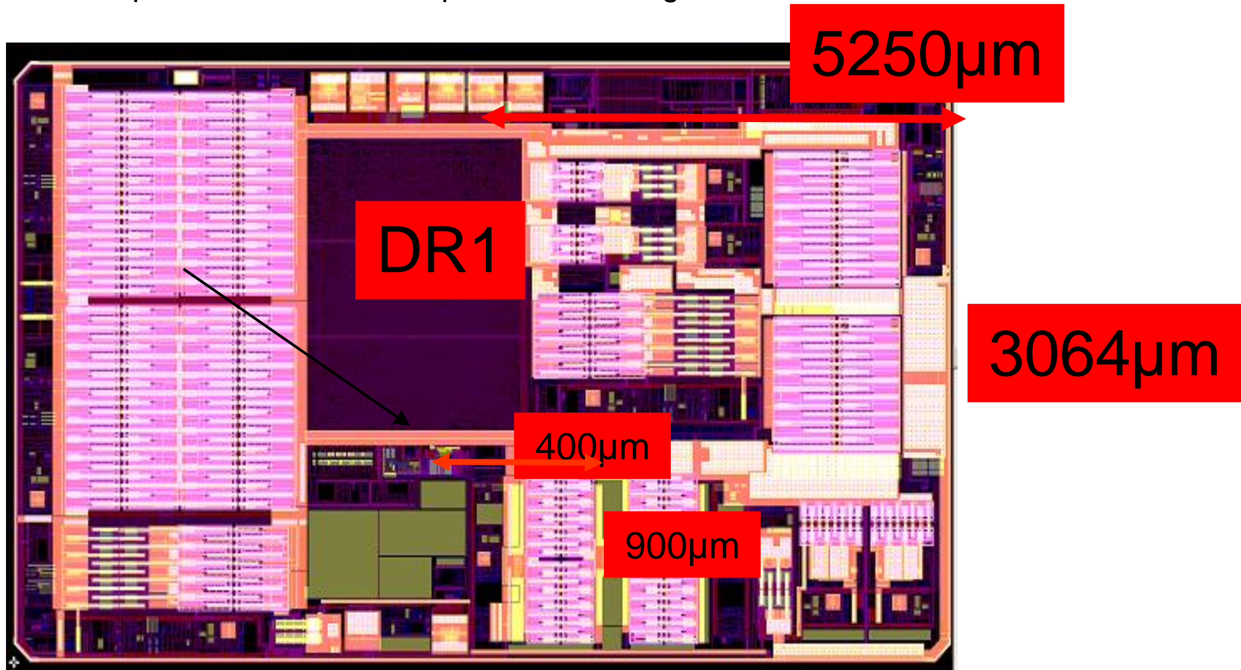


Fig. 2.7: Floorplan of the test chip.

For testing the PTM, as well as the PTM-ET solver (see next section), the part of interest is the one found as DR1 in Fig. 2.7. In Fig. 2.8 a zoom-in to this part is shown. In Fig. 2.9 the metallization stack is illustrated.

The top view is showing the poly fingers and the width of one finger is 152.7 µm. Every pocket contains 8 fingers, so 16 channels. The total width of one pocket

equals 2443 µm. Moreover, there are 20 pockets and the effective area is (152.7*2) *(68 *10) = 0.208 mm^2.

The test conditions for the device of interest DR1 are:
During the short circuit test the driver in question sees the following biases: 0V on source and 14V on drain. The gate is controlled by an external circuit, VGS is 1.63V. The current ID will be limited to approximately 3A. The power is expected to be 42 Watts at the beginning, but then due to self-heating the power decreases.

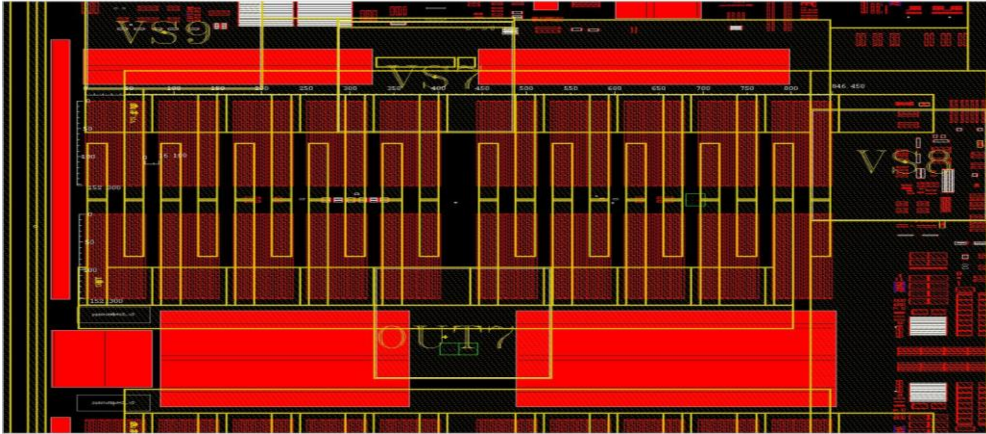


Fig. 2.8: Zoom-in to the section DR1.

The timing of the pulses on the drain is: On time 118us, period 500us, duty cycle 23%. Stop these repetitive pulses at 300ms (first cycle). The desired output of the test is:

- Simulation of total RDSON of the driver + interconnect,
- Mean time to failure figures (electromigration),
- Transient dynamic 2D (or 3D) of the temperature distribution on OUT7, and the gradient to the neighboring devices according to the specified bias and power condition,
- Current Density distribution in all metal layers,
- Simulation of the self-heating of the metal tracks,
- Simulation of the thermally induced mechanical stress.

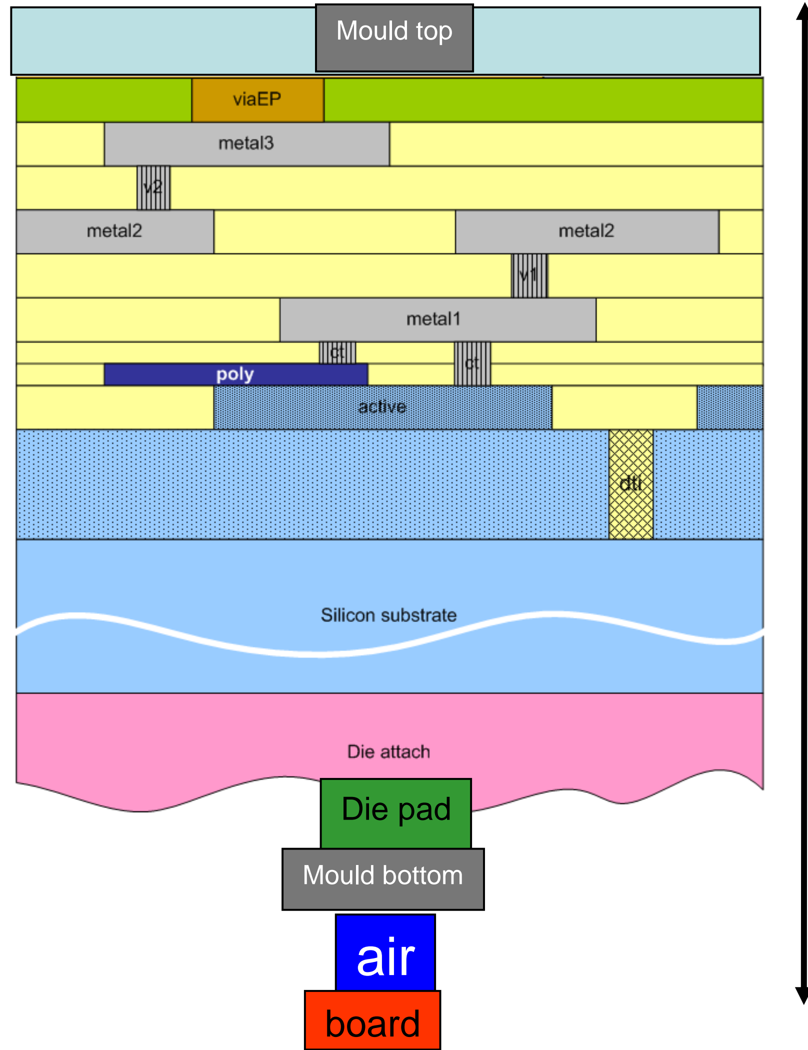


Fig. 2.9: metal/via stack of the back-end.

2.3 *Test case 3 – Smart power driver test chip with thermal sensor*

The next test case represents a realistic industrial smart power driver with a build-in thermal sensor. This test case allows to dynamically measure the temperature of the driver and also takes the impact of a package and the substrate into account. It is a good test case to evaluate the dynamic responses of the electro-thermal solver in strong coupling mode as well as in co-simulation mode.

The smart power driver was developed as a stand-alone driver in a testchip. It consists of a 45V NLDMOS of which drain, source and gate terminals are made externally accessible through bondpads. Additionally, a thermal sensor is embedded into the testchip, to allow measuring the dynamic temperature over time. This sensor is also made accessible through bondpads.

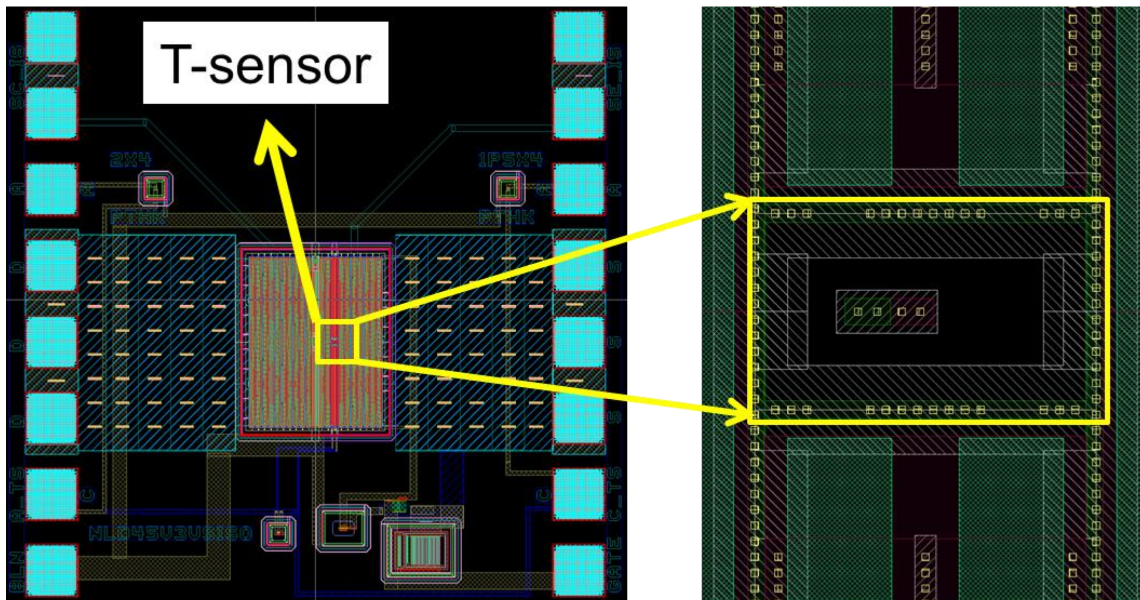


Fig. 2.10: Smart power driver testchip, using a 45V NLDMOS

The smart power testchip was developed and fabricated. First silicon arrived in September 2014 and was submitted for assembly. Ceramic packaged devices have been used at ON Semiconductor to perform first measurements on the power driver. The driver is confirmed to be functional and shows the expected I/V characteristics. The picture below shows the typical device characteristic measured at room temperature.

As next steps, ON Semiconductor will measure the power device under transient conditions and monitor the temperature evolution over time. This measured data

will later be compared to the simulation results as generated by the Magwel electro-thermal solver. Short pulses will be used to exclude the contribution of the package while longer pulses will be used to also confirm the simulation results when a package effectively contributes to the heat flow.
In a cooperation between ON Semiconductor and the Technical University of Brno (BUT), also BUT will perform pulsed measurements on the smart power driver. Objective is to reuse the measurement setup as was built to evaluate the bondwires and to apply bursts of pulses to the smart power driver and to try to extract device reliability limitations, thermally induced cracks and possibly ageing effects.

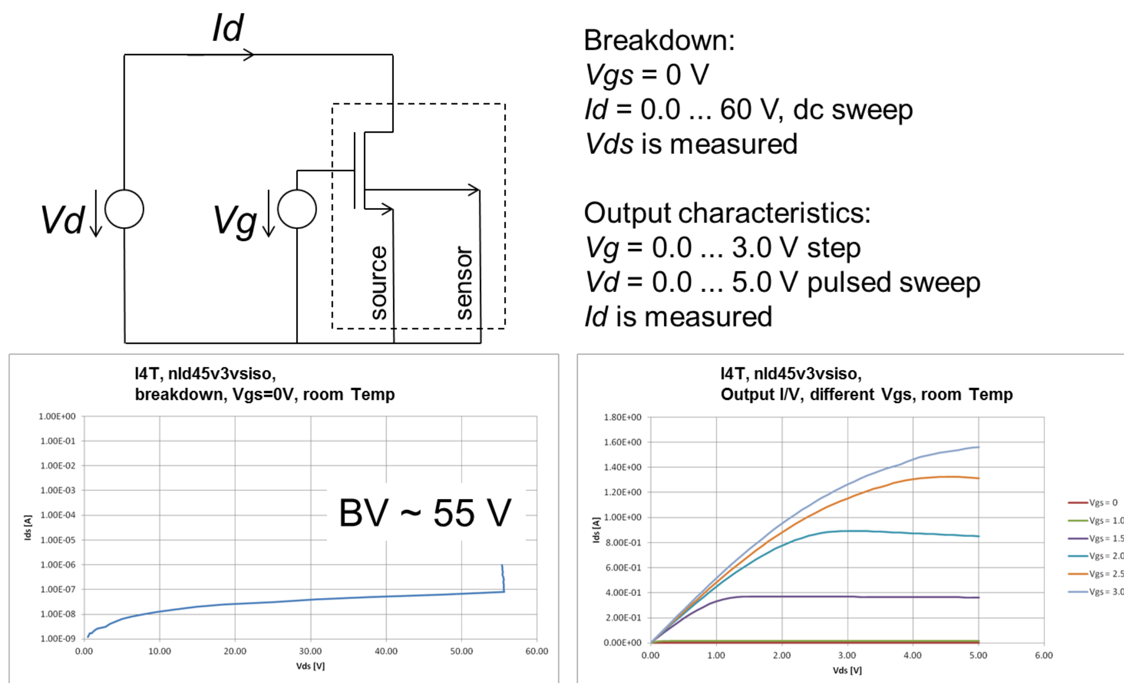


Fig. 2.11: DC BV and I/V characteristic of the Smart power driver

2.4 *Test case 4 – An 8-shaped inductor*

The 8-shaped inductor of NXP Semiconductors (see Fig. 2.12) is an excellent test case to demonstrate the quality of the software for EM solving. It represents the state-of-the-art at the end of the ICESTARS project [Date-2012] and therefore any progress obtained in the present project must guarantee that no degradation of tools occurs while developing novel algorithms. This is not an idle task: between the ICESTARS and the nanoCOPS project, the Magwel solver has been upgraded with several algorithms to deal with the solving of large sparse system in the transient regime.

We summarize here the major modifications:

- The Magwel solver has a built-in scheme to use a hybrid direct/indirect solving strategy for handling large sparse systems.
- An upwinding scheme for the Maxwell-Ampere equation has been implemented.
- Current boundary conditions can be imposed on the Magwel solver.

In order to demonstrate the progress achieved within nanoCOPS we will compare the computation times of the inductor in stand-alone mode as well as the use model based on a strongly coupled device-circuit simulation mode. The latter will be done using the Magwel kernel combined with the transient time integration methods for which a prototype implementation was done in the ICESTARS project but that was not pushed to an application on industrial sized layouts yet.

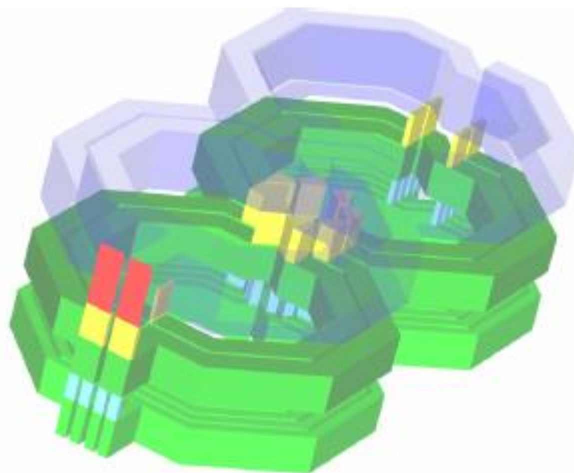


Fig. 2.12: View of the 8-shaped inductor from above. The vertical direction is stretched.

2.5 *Test case 5 – A fast and reliable model for bondwire heating*

This test case deals with the development and validation of a fast and reliable model for the calculation of the temperature distribution in bondwires, and thus the determination of the maximum allowable current for its posterior dimensioning as requested by partner ON Semiconductor. The model will permit to take into account the parameters (i.e., moulding compound material and dimensions, bondwire characteristics, etc.) that geometrically define a package. To validate our model, results will be compared with those obtained through high-fidelity computer simulations of a realistic configuration, as illustrated in Fig. 2.13 taken from [TAV-2000], and measurement data, if available.

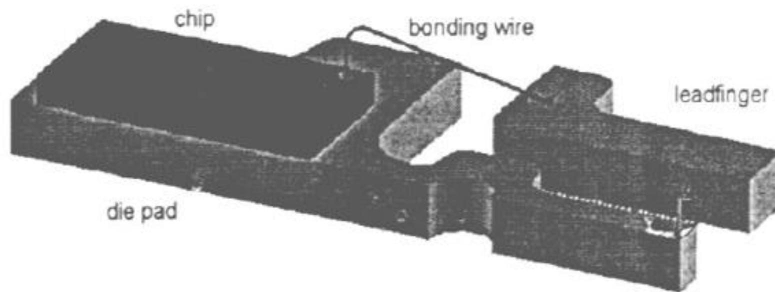


Fig. 2.13: Bondwire test case configuration showing its main components.

In the smart power electronics industry, bondwires play an essential role in predictive simulation of electro-thermal coupled problems. The reasons are that bondwires often create reliability limitations and depending on its length and diameter also can determine the boundary conditions of the ET solver. Without assessing for reliability issues and without properly setting the boundary conditions the simulation results are "void".

In general the bondwire is found between a die and lead finger.

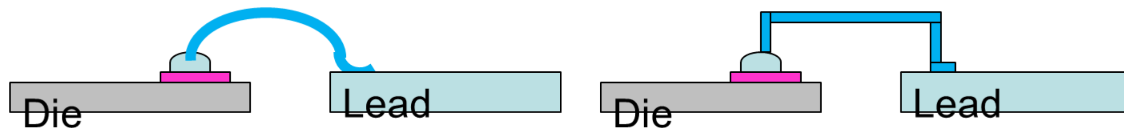


Fig. 2.14: Left panel: real bondwire. Right panel: idealized shape bondwire to deal with meshing issues or to convert to 1D characterization.

In order to allow the end-user to set the bondwire characteristic variables and to assess the related reliability, ON Semiconductor defined a first draft version for a GUI. The most relevant requirements are listed below:

GUI definition:

- Wire length:
  - A real bondwire makes an arc, not a straight line from pad to lead. The real length is therefore longer compared to the distance from pad to lead. The GUI needs to allow to set the “real” wire length, which could be different compared to the drawn wire length.
- Wire diameter:
  - The GUI needs to allow setting the wire diameter, typically in “mils”.
- Wire type:
  - The technology file needs to allow to define multiple wire materials (Au, Al, Cu, AuPd,…) and hold the electrical and thermal material constants for this.
  - The GUI needs to enable selecting a wire type
- Bondpad temperature:
  - Will dynamically vary and needs to be thermally coupled with the bondwire model. The wire temperature is important to predict reliability, as well as fusing conditions and to correctly calculate the local temperatures. Placing the wire physically in the layout is the best way for a user to create this model-interface. It means that the GUI needs to allow placing the bondwire.
  - **Issue:** 99% of bondwires are placed non-orthogonally, while the electro-thermal simulator of Magwel expects orthogonal shapes for meshing.
  - **Solution:** Just draw a line that represents the bondwire and do not embed any real shapes or meshes into the solver, but calculate the wire “hidden” by using a model.
- Proximity:
  - It is important to be aware of proximity effects, e.g. a bondwire will be impacted by the presence of other wires nearby. This will affect the thermal properties. If wires are drawn on the layout view, also proximity can be extracted from that drawing
- Thermal profile:
  - During its full life time, a product will operate under variable environmental conditions. A thermal profile defines how much time a product has operated biased, unbiased or in standby in a given temperature range. Under bias, current and temperature affect the ageing of the bondwire and bondwire interface, while unbiased mainly temperature keeps ageing the bondwire interface, and much less the bondwire itself.
  - Also mold is ageing by temperature and time. The table below shows a typical example of a thermal profile.

Biased		Unbiased	
300h	180 degC		
1000h	170 degC	1000h	150 degC
4000h	150 degC	10000h	125 degC
10000h	125 degC	50000h	<85 degC

The GUI needs to allow the setting and to easily vary a thermal profile, biased and unbiased. This allows the user to quickly assess which parameters are most critical and how much change is required to improve to acceptable levels. For the GUI we propose to add 2 spin buttons "dTime" and "dTemp", which add a delta to all time or temperature values in the thermal profile.
Issue: The thermal profile includes multiple temperatures, while PTM-ET will typically simulate at 1 ambient temperature.

- Interactive GUI interface:
  - The GUI needs to allow changing the wire properties (wire length, diameter, double wire, wire type), and "approximately" recalculate the bondwire and life time without rerunning the PTM simulation.
  - The GUI needs to show warnings and errors if life times are endangered.
  - In the technology file, life time models can be formulated by Black's equation or by a set of table models, representing measured data.

To extract reliability data, a test plan was defined between the Technical University of Brno (BUT) and ON Semiconductor. ON Semiconductor focusses on steady-state measurements, while BUT focusses on pulsed measurements. Definitions of tests have been defined and exchanged and BUT performed the first transient measurements.

The Technical University of Darmstadt has developed an analytical electro-thermal model for the bondwire. ON Semiconductor specified the input and output requirements for the model. Actually, a data format reduction algorithm was agreed upon, to strongly reduce the data file sizes and now the measured data is exchanged. The next objective is to correlate measured and modeled data and to improve the model where needed to well reflect the measurements.

The picture below clarifies the links between the bondwire use case and the smart power driver use case used and how they link to ET coupled problems and reliability:

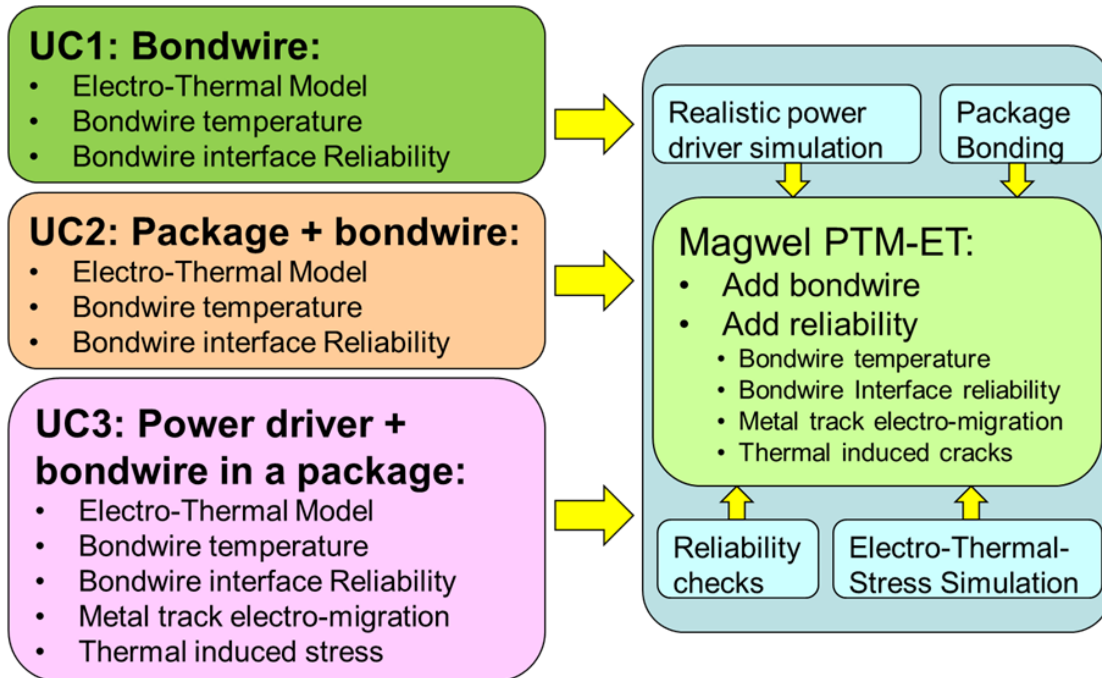


Fig. 2.15: Links between bondwire, reliability and power driver use cases to extend and validate the Magwel electro-thermal PTM-ET simulator.

Starting from a bondwire model, specified by ON Semiconductor, and developed by the Technical University of Darmstadt, and measured by the Technical University of Brno (BUT), model and measurements data are extracted and compared. The bondwire temperature is further used to predict reliability risks like bondwire fusing, mold compound degradation (due to hot bondwire) and bondwire interface reliability.
The bondwire GUI and bondwire model are used by Magwel to implement a bondwire as an electro-thermal compact model into PTM-ET, but also to predict the related reliability risks.
The bondwire assembled in a package will be used as a use case to evaluate the bondwire model implementation into PTM-ET. This case is simple yet complete enough to validate all the interactions between the bondwire model and the meshed parts in the electro-thermal solver.

As a final step, the smart power driver with bondwires assembled in a package is used as a more complex and industrial representative use case to evaluate the GUI, the bondwire model, the reliability warnings and the electro-thermal simulation capabilities of the most complete revision of PTM-ET.

2.6 *Test case 6 – RF and electro-thermal simulations*

This test case of ACCO Semiconductor represents a realistic stand-alone power stage used in an actual Power Amplifier (PA) product. The driver stage has been removed to facilitate electro-thermal retro simulation. In order to measure the transistor junction and the board ground pad temperature, two thermal sensors (diodes) have been integrated. This allows to extract junction to case (Rjc) and case to ambient (Rca) thermal resistances. All input and output matching networks are integrated on the PCB board.

To evaluate the package and substrate thermal impact on RF performances, two test boards have been realized. On the first one, to optimize the heat flow, the test chip is directly mounted on the PCB. On the second one, the BT substrate (4 copper layers) is inserted between the die and PCB (see Fig. 2.16). All the junctions between PCB, BT and the test chip are made by bump pads.

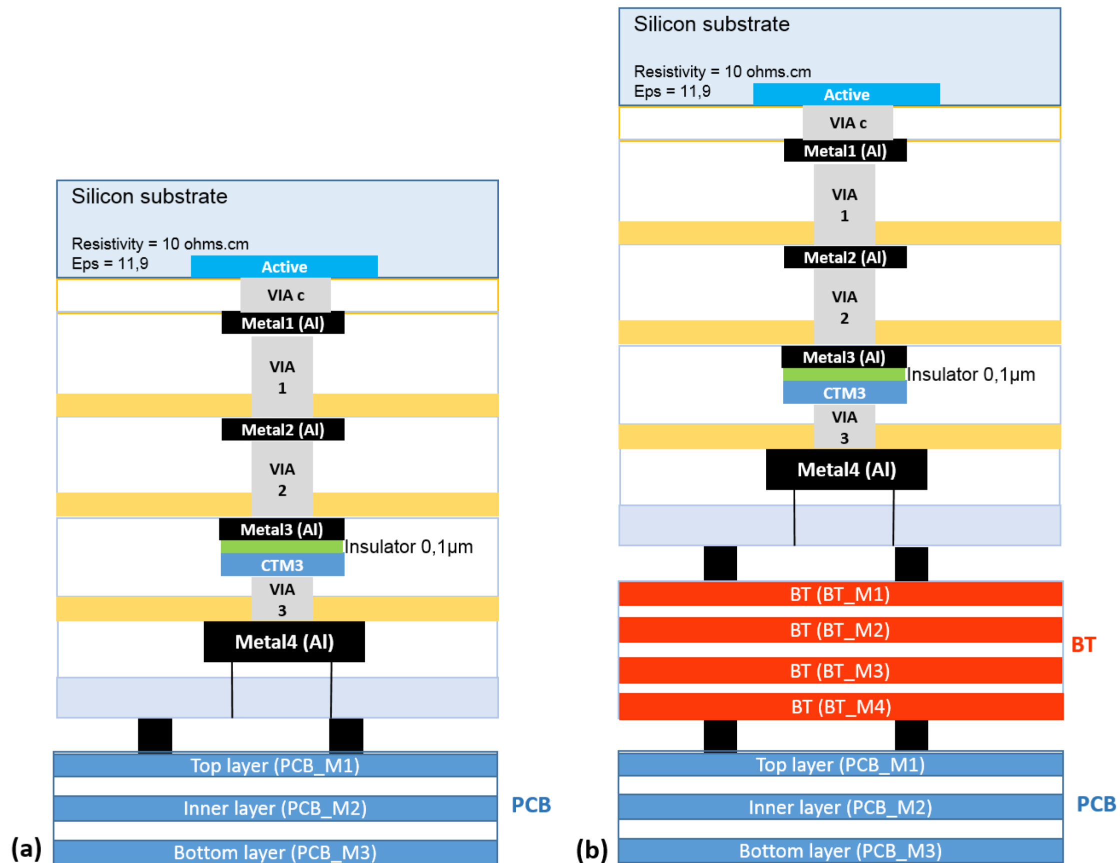


Fig. 2.16: Power stage test boards. Si die mounted (a) on PCB and (b) on PCB plus BT substrate.

The stand-alone RF power stage is realized on a 0.18µm standard CMOS technology. Designed for band II (@ 1.9GHz) it delivers on board 26dBm linear output power (@-40dBc) with 44% efficiency.

The silicon die, PCB and BT substrate were developed and fabricated. Measurements are available and have been done at room temperature with different Si dies to evaluate the impact of the process variation on RF performances. RF measurements confirmed the test case functionality, the target specifications and performance reproducibility.

In the next phase, ACCO Semiconductor will start the retro simulation. The goal is to evaluate and validate Magwel's electro-thermal solver in terms of accuracy, memory and time simulation. To complete this simulation phase, results will be compared with Keysight's electro-thermal simulations.
Parallel to that activity, in a cooperation between ACCO Semiconductor and the Technical University of Brno (BUT), the BUT laboratory will redo and hopefully confirm previous test case measurements done at room temperature and will pursue PA cell measurements at different ambient temperatures and under VSWR.

2.7 *Test case 7 – Reliable RFIC Isolation*

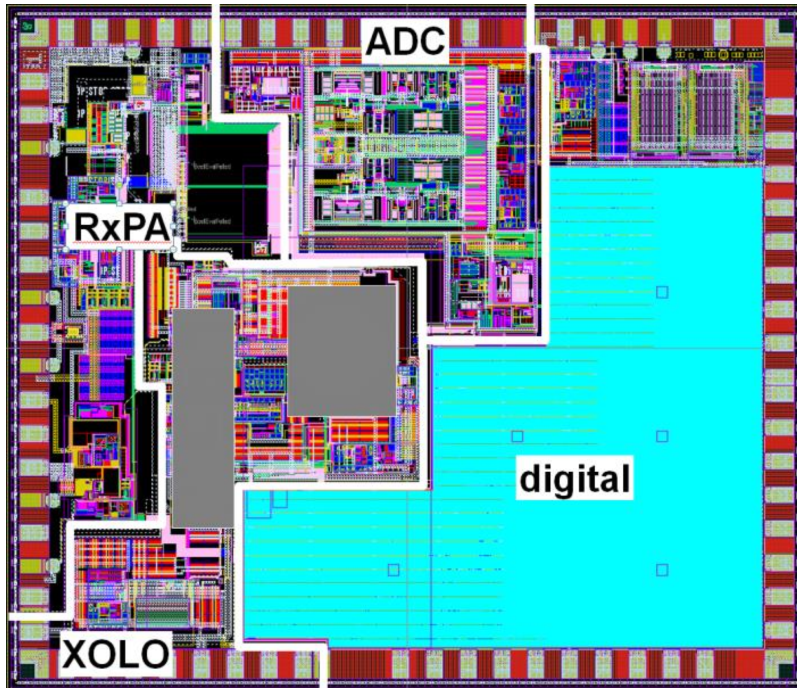


Fig. 2.17: Integrated RF-CMOS automotive transceiver design

In order to minimize interference issues and coupling effects in RF products, it is essential to apply proper floorplanning and grounding strategies. The interaction of the IC with its physical environment needs to be accounted for, so as to certify that the final packaged and mounted product meets the specifications. This test case has been provided by NXP Semiconductors.
The first focus is on the key requirements to address physical design issues in the early design phases of complex RF designs. Typical physical design issues encountered, such as on-chip coupling effects, chip-package interaction, substrate coupling and co-habitation, have been investigated.
The main challenges are the first order prediction of cross-domain coupling. Therefore we apply a floorplan methodology to quantify the impact of floorplanning choices and isolation grounding strategies. This methodology is based on a very high level floorplan EM/circuit simulation model, including the most important interference contributors and including on-chip, package and PCB elements, to be applied in the very early design phases (initial floorplanning).

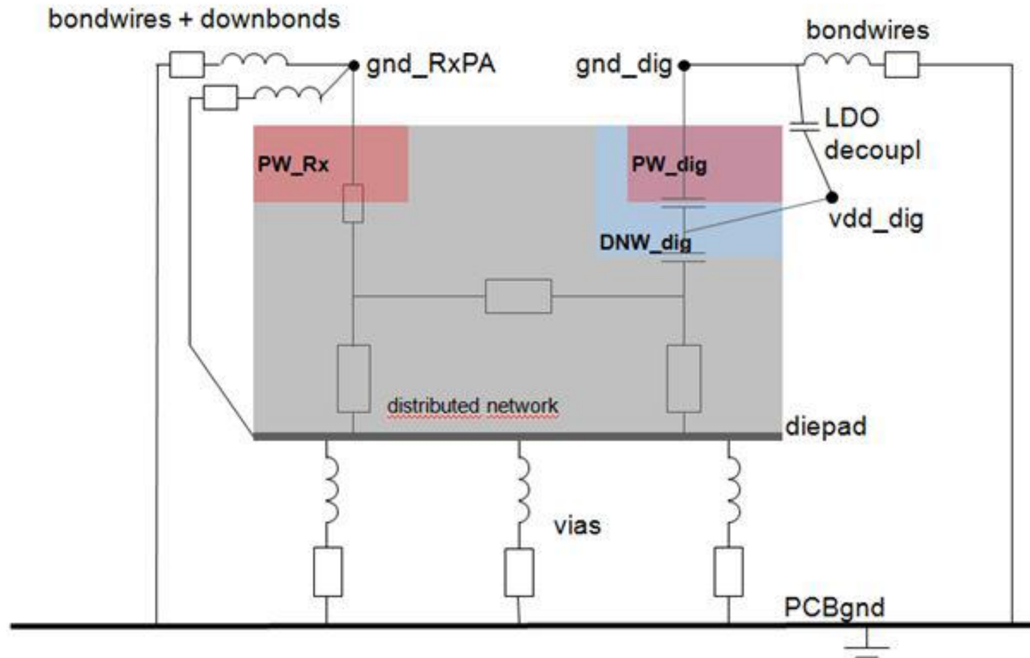


Fig. 2.18: Floorplan model for isolation and grounding strategies

The overall model of a complete RF product contains the following parts (see Fig. 2.18):

- On-chip: domain-regions, padring, sealring, splittercells, substrate effects.
- Package: ground and power pins, bondwires/downbonds, exposed diepad.
- PCB: ground plane and exposed diepad connections.

The effect of the number of parameter variations on the impact of noise from digital parts on the isolation sensitive RF domains will be investigated, i.e., the number of downbonds, the number of ground pins, the domain spacing and shape, the application of deep-Nwell and exposed diepad, and the number of exposed diepad vias. Some measurements are available and can be compared with.

2.8 *Multirate circuit examples*

The simulation engines for multirate circuit simulation will be tested against a decent benchmark library. The library will be completed during the course of the project by circuit examples from partners, third parties and own developments. The next subsection gives a table of the benchmark circuits available from the partner FH Oberösterreich (FHO).

2.8.1 Table of benchmark designs

The circuits are available to other partners both as a schematic as well as a C++ class model. The device models used include standard Spice models, BSIM, VBIC, models as well as selected models from the partner NXP Semiconductors (MOS9, MEXTRAM). The circuit classes are focused on oscillators with high quality factors, mixers in the up- and downlink and amplifiers with multitone excitation.

LNA test example
The transAmp is a wide-band low noise amplifier (LNA) in transimpedance topology in 0.25µm RF-CMOS design. For simulation, the transAmp amplifier is embedded in a testing environment using an external bias tree and input and output modelled as PORT sources, i.e., a voltage source in series with a resistor (or a current source parallel to a resistor).

Mixer example
The c9linmix mixer is a simple single-ended version of a Gilbert mixer (enhanced by a cascade stage to yield better linearity) for GSM in 0.25µm standard CMOS.
For GSM usually the RF input frequencies lie in a frequency band from 925 MHz up to 960 MHz. To down-convert an input signal to the band of a low-IF receiver, the LO frequency must lie very close to the RF input frequency ($|f_{lo} - f_{rf}| < 1$MHz). Furthermore, the bandwidth of the GSM channel is about 200 kHz, consequently, for intermodulation distortion computations, a second input frequency must lay within this distance. However, displaying simulation results based on such close frequencies is not instructive. Therefore larger distances between the different frequencies may be chosen for reporting purposes. Note that the RF input source is a source of type PORT, i.e., a voltage source in series with a resistor. The parameters of such a source should be chosen according to the purpose of the simulation.

Voltage controlled oscillator
The vcoBi oscillator is a simplified version of a fully integrated 1.3 GHz LC-tank VCO for GSM in 0.25µm standard CMOS. The VCO is tuneable from about 1.2 GHz up to 1.4 GHz and has a very low phase noise of less than -130 dB at 1 MHz offset from the carrier frequency. For simulation, the oscillator is embedded

in a testing environment using a virtual output buffer load and tuning voltage as well as core current modelled as independent DC sources.

Example	
transAmp	x
c9linmix	xx
vcoBi	x
vcoBi+ Mosfet model	x
LNA model	x
IQ Modulator	xx
IQ Demodulator	xx
QPSK receiver	x
PLL	x
PA	x
Colpitts oscillator	x
Pierce oscillator	x
VHF oscillator	x
Driscol oscillator	x
Schmitt Trigger	x
Gilbert cell mixer	x
Low voltage mixer	x
Single balanced mixer	x
Folded switching mixer	x

Table 2.1: Validation coverage of development tasks with available test cases (x = baseline test case, xx = possible additional test case).

Quartz crystal oscillator (Colpitts)
This is a standard Colpitts oscillator circuit operating at 20 MHz in bipolar technology. The crystal is replaced by a series of RLC and a capacitor in parallel representing the package.

PLL Design
The PLL design was designed for the ISM band at 5.8 GHz with a tuning range between 5.6 and 6 GHz. 85 channels can be allocated with a channel bandwidth of 150 MHz. This design is described in [SIAM-2015] in detail. The frequency

divider chain of the design divides the frequency in 5 stages of ratio 2 from approximately 1MHz to approximately 31.25 kHz. The Figure below shows the input signals for different stages in the divider chain. Especially the huge spread of the frequencies in the divider chain is highly challenging for multirate methods.

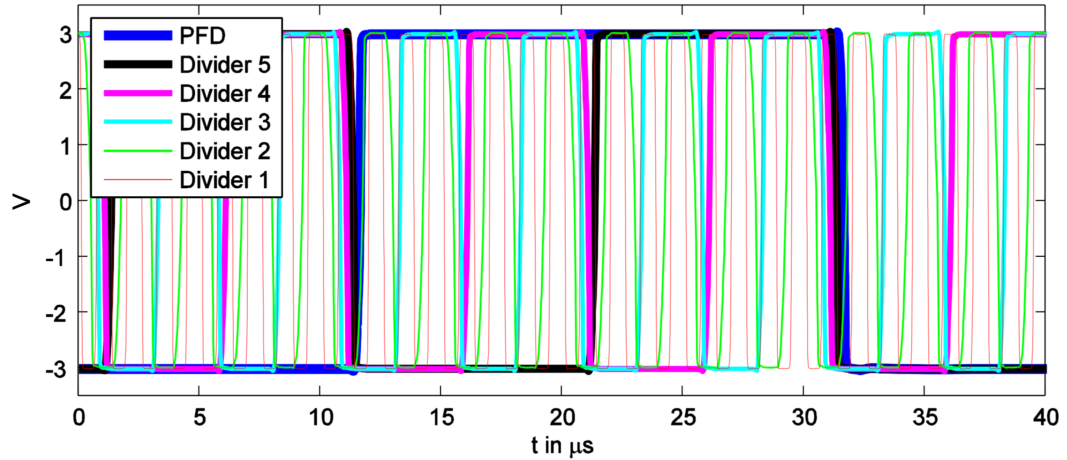


Fig. 2.19: Several signals in a frequency divider chain as part of a PLL

Planned designs: For tests of the linear interface to the Magwel device simulator RF filters in stripline or microstrip technology are considered and planned for year 2 of the project.

3 Validation plan description

The validation plan will be based on the test benches/examples, as described in D3.1a, "Tool Development Test Set", which gives coverage of the complete functionality of the tools to be developed. This will give a rough description of when and what in terms of validation, including test benches and timing.

There is a distinction between validation in the development phase and final validation of the algorithms at the end of the project, where we will use a few larger/more complex test cases.

Accuracy of the MOR algorithm can be validated in both time domain and frequency domain for linear models. Accuracy of the MOR algorithm can be validated in time domain for nonlinear models. For linear models, passivity and stability can to be validated, if necessary. For nonlinear systems, stability is hard to be preserved by the reduced-order model, thus this may not be validated.

Status of test cases

Test case	**Uploaded**	**Expected upload**
Test case 1 – A realistic size power MOS at constant temperature	Yes	
Test case 2 – A realistic size power MOS in ET coupling mode	Yes	
Test case 3 – smart power driver test chip with thermal sensor	Yes	
Test case 4 – An 8-shaped inductor		Q1 2015
Test case 5 – A fast and reliable model for bondwire heating	Yes	
Test case 6 – RF and electro-thermal simulations		Q1 2015
Test case 7 – Reliable RFIC Isolation		Q2 2015

Table 1: Status of test cases uploaded on the webpage

3.1 *Work package 1 validation*

The activities in WP1 "Time-domain Simulation of Coupled problems" cover the development of new techniques that efficiently deal with multi-dynamics, by multirate (multi-timescale, envelope) and co-simulation, and exploits pMOR (parameterized MOR) techniques. New methods for studying thermally induced ageing effects will also be developed.

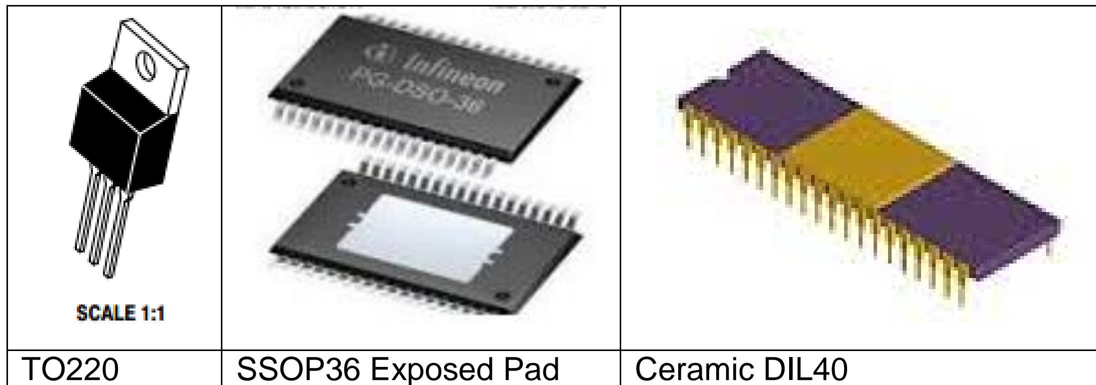
An interesting application of MOR is to replace field-defined systems by reduced systems. The underlying idea is that the field equations in a way can be viewed as circuit equations with the notion that the circuit elements correspond to mesh links and nodes. Of course such circuit schemes are far too large to be submitted to circuit simulation tools such as SPICE or Spectre. However, if ROM can be applied successfully to such field-derived netlists, circuit simulation may come within reach. In order to validate this approach we have identified a route to merge ROM output into Spectre circuit simulation. First the field equations are presented as state-space equations. Next these equation are submitted to ROM in order to compute reduced A, B, C, D matrices. The final step is to submit the reduced matrices to Spectre.

In circuit-device-EM coupling, two distinct interfaces between the circuit simulators from HUB and FHO have been defined. For devices with a linear characteristic, the Jacobians of the static and dynamic contributions are required only once and can be incorporated into a circuit simulator quasi as a linear subcircuit. Hence the coupling between the simulators is only required once before the transient/envelope simulation. The implementation is already performed and tests are ongoing.

The purpose of the validation is to demonstrate that it is feasible and useful to replace the package by a compact-model representation using ROM. The compact model is obtained using algebraic means, e.g. starting from field solving, applying ROM and resulting into effective input to Spectre.

For driver applications mainly 3 packages will be considered.

1) For discreet power FET devices, a TO220 package is quite commonly used. This package consists of a metal plate on which the die is soldered and where the die is covered in a box of mold compound. This type of package is often mounted on a cooling plate to extract heat from the die.
2) For the industrial test case 2, a plastic SSOP16 package is used with exposed pad. The dies and bondwires are embedded in mold and through an exposed pad heat is extracted from the die. The package is depicted below.
3) For industrial test case 5, a ceramic DIL24 package is used. In this package the upper side of the die and bondwires resides in free air while the heat is still extracted from the bottom of the die towards the paddle. Also this package is depicted below.



TO220	SSOP36 Exposed Pad	Ceramic DIL40

In contrast, an interface for incorporating nonlinear devices requires, for a strong coupling at any Newton iteration and any distinct time, the Jacobians and the right hand side for the static and dynamic parts separately. Therefore, strong coupling requires a continuous exchange of data between the simulators. A prototype interface has been developed by MAG and is on test by HUB.

3.2 *Work package 2 validation*

The activities in WP2 “Uncertainty Quantification” cover the development of new techniques for coupled problems and possibly large deviations, which can deal with a high number of parameters. Therein, parameterized MOR techniques for UQ and stochastic modelling shall be applied. The UQ will be extended to determine variability and reliability.

The parameterized MOR techniques to be tested at least include the pMOR method based on multimoment-matching from [MSA-2014], and its application in UQ analysis including the Monte Carlo scheme and the stochastic collocation method.

The solution of stochastic models will mostly rely on stochastic collocation techniques or other sampling techniques, where deterministic coupled problems are resolved for specific realizations of the random parameters. Thus the same problem type appears as in WP1 “Time-domain Simulation of Coupled problems”. Consequently, the validation, which is used with respect to WP1, can also be considered for the coupled problems in WP2.

A validation on the level of the stochastic models is more critical. The measurements represent a data set of different properties for each realization of a technical device. The values of the properties can be partitioned into input parameters and output parameters of the underlying deterministic models. In the stochastic models, variations within the input parameters are described by random variables or random processes. Probability distributions have to be predetermined for the input parameters. For a validation, the measurements of

the output parameters can be applied to reconstruct simple statistics (for example, mean value and sample variance), which are compared to the statistics obtained from the simulation of the stochastic model.

Concerning the construction and calibration of probability distributions for the input parameters from measurement data (task T2.6), a validation could be performed as follows. Assume that a probability distribution has already been fitted to some training data set. For validation, statistics (for example, moments) obtained from this probability distribution can be compared to statistics resulting from an additional validation data set. However, if a disagreement appears, then the validation data set can be merged with the training data set and the fitting technique is repeated. Hence the updated probability distribution includes the statistical behavior of the former validation data set now. A further validation would require an additional set of measurements. Thus the procedure can be repeated.

In general, for electrical parameters, measurements can be provided by On Semiconductor, NXP Semiconductors and ACCO Semiconductor, as well as by Brno UT. For geometrical parameters all industrial partners rely on the information provided by the foundries, who provide (low, nominal, fast) triples. These are used in Worst-Case-Corner-Analyses (WCCA). The Uncertainty Quantification techniques in WP2 will compare results from Stochastic Collocation with Monte Carlo and with WCCA. The techniques in WP will be checked if they can assist in identifying non-trivial corners in WCCA.

For several problems (like RFIC) some parameters of interest still have to be identified.

4 Measurement setup

After the first meeting between ONN (ON Semiconductor) and BUT (Brno Univ. of Technology), the first partner proposed a task on the measurement of the bondwire dynamical fusing. Partner ONN fabricated test chips (SOIC package so far) where the individual bondwires with different lengths, diameters and materials have been encapsulated. Partner BUT has been asked to prepare a complete methodology and experimental setup to do such investigations.

After summing-up all necessary requirements and parameters to be achieved, BUT decided to utilize the National Instruments internal PCI card 6251 supplemented by a professional interface. This device comprises of two analog outputs; only a single channel is used at the moment for arbitrary pulse driving signal generation. The eight bit digital port is used as follows: three bits are dedicated for multiplexing the individual bondwires, two bits directly control the gain of the first programmable gain amplifier (PGA), two bits adjust the gain of the second PGA in a cascade and the remaining bit signalizes if the measurement sequence is forwarded to the test board. For capturing the necessary analog signals, two channels with 10 bits resolution A/D converters are used. Referring to this concept, the experimental setup can be divided into two parts, namely the software, which directly controls this PCI card, and the PCB, with practical implementation of the multi-channel switching power source.

4.1 *Software part for bond wire tester*

The software part of the project consists of two executable Matlab scripts with a graphical user interface (GUI). The first one is called *Generator.m* and creates a text file with the analog driving signal. The driving force can be derived for non-inverting as well as inverting MOSFET drivers. Up to nine bursts, with an arbitrary time window and duty cycle, can be created with cooling time delays placed between these bursts, see Fig. 4.1 for example. The test sequence has no time scale; this parameter is variable and is included into test data just before the procedure of the measurement itself. Nevertheless, to easily visualize the test sequence in some suitable program (Matlab, Mathcad, Microsoft Excel, etc.), the time vector can be included as a part of the saved file (first column).

The generated file can then directly be loaded by the second program *Measurement.m*, which is capable to do the rest, i.e., choose a bondwire to be measured and specify the power voltages for the individual measurements. A sampling rate of the PCI card allows a single pulse width scaled down to 1μs, while the upper boundary is arbitrary; in fact, it can be boosted up to DC. The program is designed for two basic measurement regimes. For the purpose of quantifying the fusing time, a single channel measurement should be activated.

Doing so, only the necessary amount of data is stored in single-column text format with reduced number precision. Recently, a progressive filtering method was performed after measurement in order to reduce the amount of data to be handled. On the other hand, for a bondwire resistivity change calculation, a dual channel method should be activated because it is necessary to precisely measure and store the current through the bondwire as well as the voltage drop across this wire via Kelvin probes. As is evident from Fig. 4.2, it is possible to measure up to six bondwires and for each bondwire up to six consequent measurement scenarios can be applied. The power voltage is adjusted automatically on a MANSON 16V / 60A switching supply via a serial port. Before the start of the particular measurement, the total gain applied on the voltage across the Kelvin contacts should be guessed and set (so far manually). A measurement setup is essential in order to correctly repeat the same measurement plan for the different wire materials (represented by the different integrated circuits). That is the reason why a “saving” icon has been added to the GUI; the setup is comprised in the text file and loaded before the start of the script *Measurement.m*. The “digital” icon is used only if the hardware part of the fusing system is debugged and its individual parts are tested. It allows for immediately sending of L or H levels towards the digital output. By sending appropriate addressing, it can also serve as an immediate cut-off driving signal from the power source in the test board. For graphing, different colors are used for each different nature of measurements.

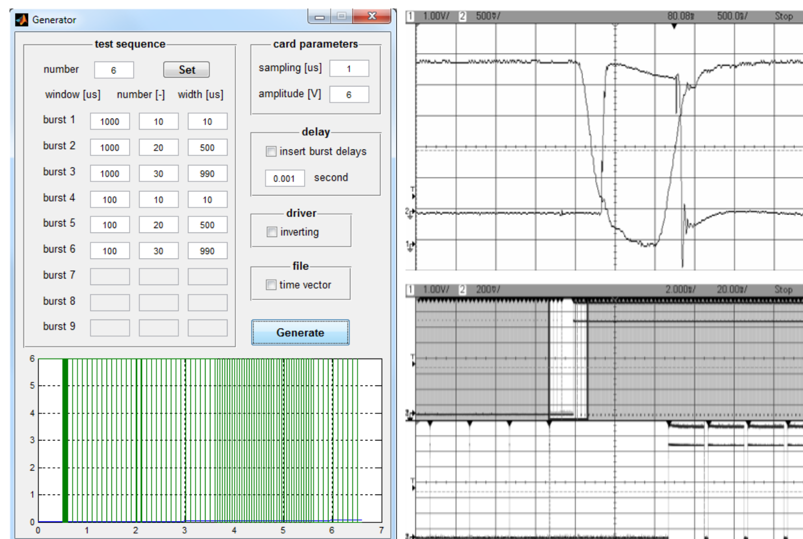


Fig. 4.1: Script for generation of the test sequence (left), oscilloscope screenshot focused on the cooling gap (lower), sharpest pulse for the inverting driver (upper).

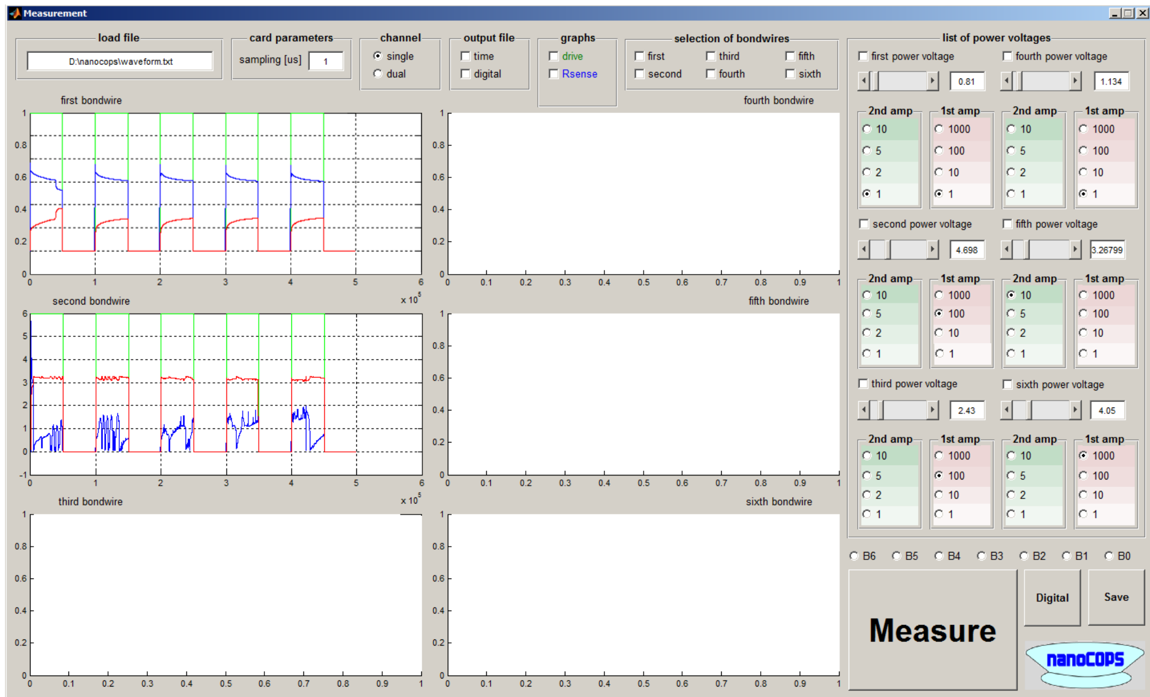


Fig. 4.2: Script for bondwire fusing measurement.

4.2 *Hardware implementation of bond wire tester*

The hardware section must reflect all demands and requirements for bondwire fusing measurements and identification of the parameters of the associated model. To briefly explain the function of the test bed, the block schematic is given in Fig. 4.3. The individual bondwires are addressed by the analog multiplexer HEF4051, i.e., three bits are used to select one power channel from six possibilities. In order to avoid failing states, all addresses set on L or H means that no power channel is selected. This conception simply means that the PCB contains six drivers, six power switches (MOSFET transistors IRFZ044) and that the same amount of amplifiers are connected to bondwires via Kelvin probes. These integrated amplifiers have differential voltage inputs and non-symmetrical output with digitally controlled gain. Since a very large final gain is necessary, a two stage cascade connection is utilized. Up to four bits can be used to set a final gain factor; these bits can be directly set via a Matlab script. For amplification of the voltage at Kelvin probes, a high-gain stage AD8253 PGA, with a gain taken from the set 1, 10, 100 or 1000, is combined with an integrated circuit AD8250, having a gain taken from the set 1, 2, 5 or 10. This control is necessary to make use of as wide a ±10V dynamical range of A/D converter as possible and to lift the signal from the noise floor but keep it below saturation. A further solution of this problem will be part of the upcoming hardware version since the software is already ready with this routine implemented. The idea behind this is to make use of the possibility to change the dynamical range of the A/D converter while

preserving the full amount of effective bits. This change will be done for a given power voltage and before a particular measurement. A very short predefined test sequence will be forwarded towards the bondwire under inspection and the necessary gain factor will be automatically calculated.

All power transistors have sources connected to a single sensing 1Ω / 50W resistor. It is advantageous since the dominant current will always come from the power branch of the active bondwire while contributions from other bondwires will be negligible.

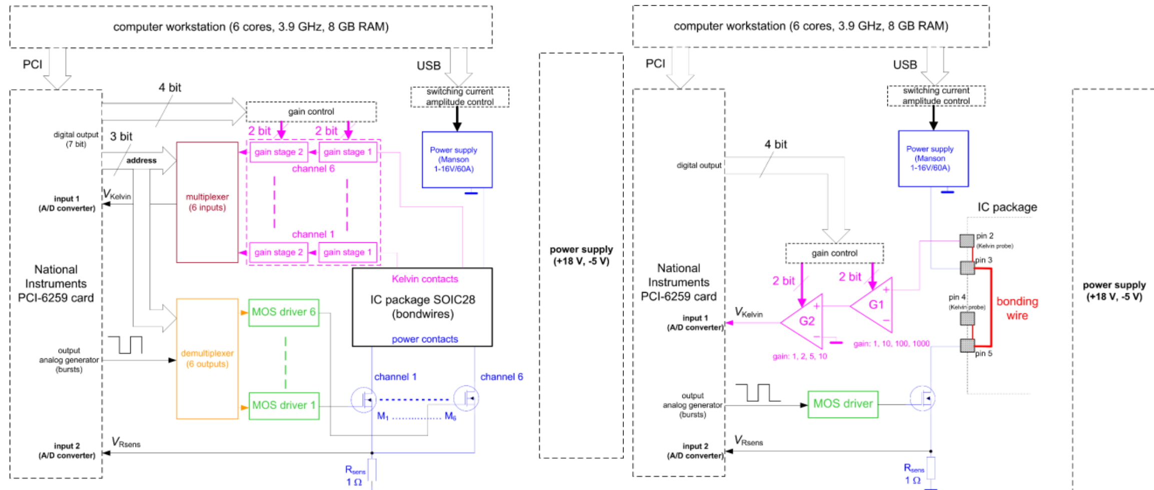


Fig. 4.3: Principal block schematics of the experimental test board (left), detailed power and signal path if some concrete bondwire is addressed (right).

A photo of the recent hardware solution evolution is shown in Fig. 4.4. Devices necessary for real-time observation and quantification of the bondwire fusing scenarios are two digital oscilloscopes (Agilent DSO-X 2012A), a power supply (Manson 16V / 60A) and a stabilized dual-channel voltage source (30V / 4A).

In order to accelerate the **ageing** process, we decided to make several tests also in the temperature cabin. Measurements are done at ambient temperature and at temperatures of 100°C and 180°C. Unfortunately, placing the integrated circuit in an oven and feed the PCB by a long bus-type cable introduces relatively large inductance causing voltage overshoots when switching on or off. This unwanted behavior can be reduced to acceptable levels by adding a two terminal RC device between drain and source of the MOSFET. The time constant for this stabber can be manually adjusted via a variable resistor.

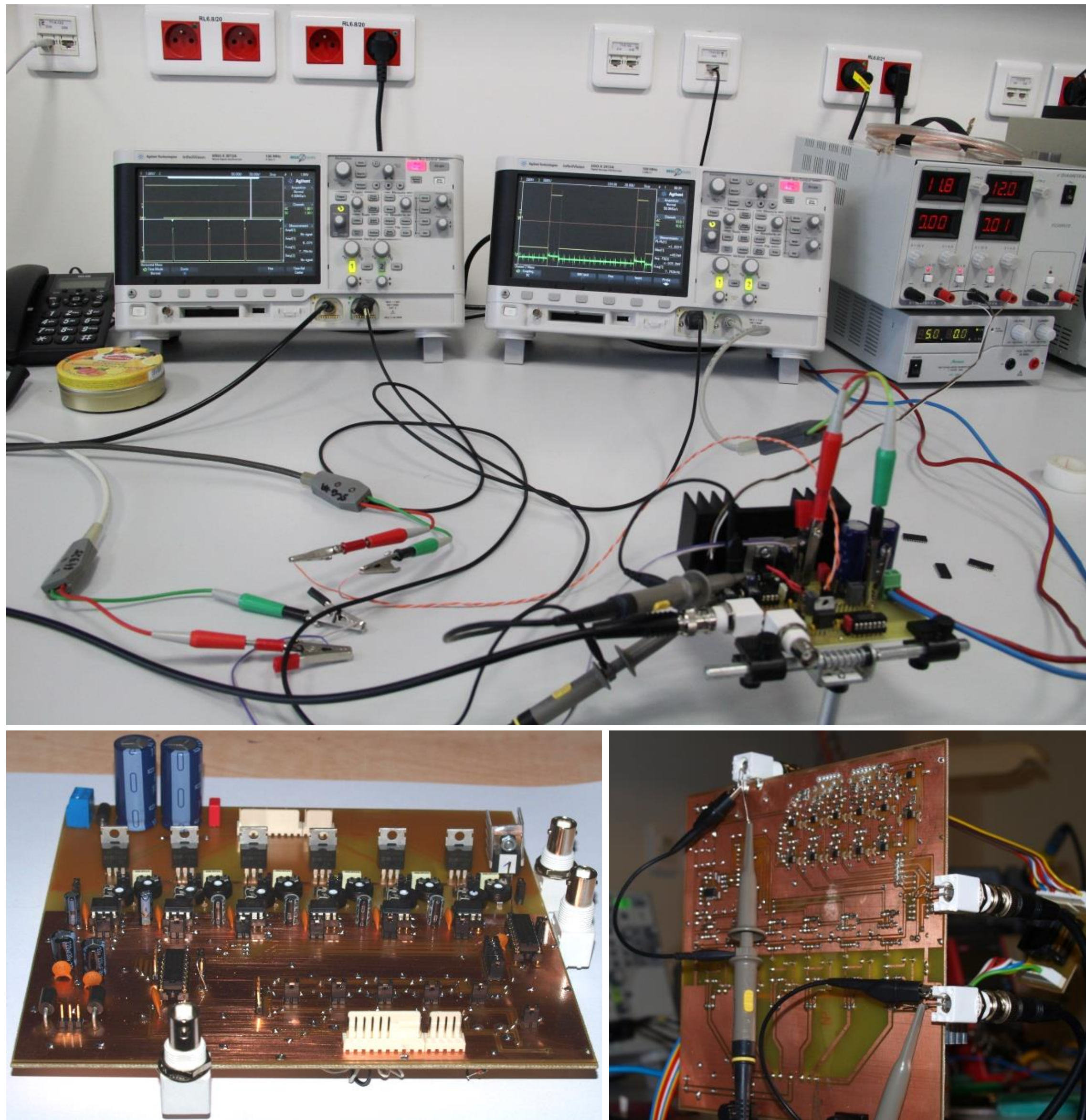


Fig. 4.4: Third (upper), fourth (left) and fifth (right) version of the experimental test board with the measurement devices.

4.3 *Experimental results of bond wire fusing*

Many integrated circuits with encapsulated bondwires have been destroyed so far, as demonstrated in Fig. 4.5. It seems that a fused bondwire does not mean an immediate open loop; various degradation processes have been intercepted by the delayed time base feature of the oscilloscopes. Few selected screenshots are given in Fig. 4.6 where a rich dynamical behavior became obvious.

DC measurements of the bondwire fusing time as a handy tool for making correlations between mathematical models and the real situation has been already done. An example of this is provided in Fig. 4.7.

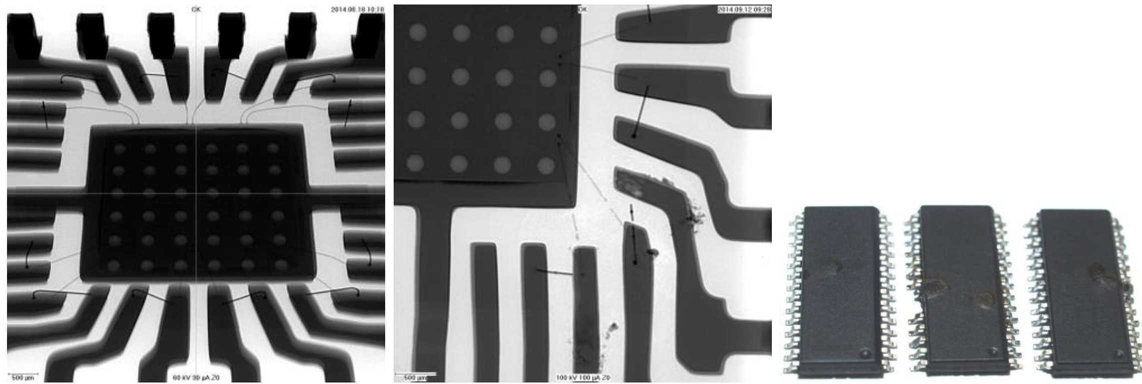


Fig. 4.5: X-rays of bondwires before (left) and after (middle) successive fusing, destroyed integrated circuits (right).

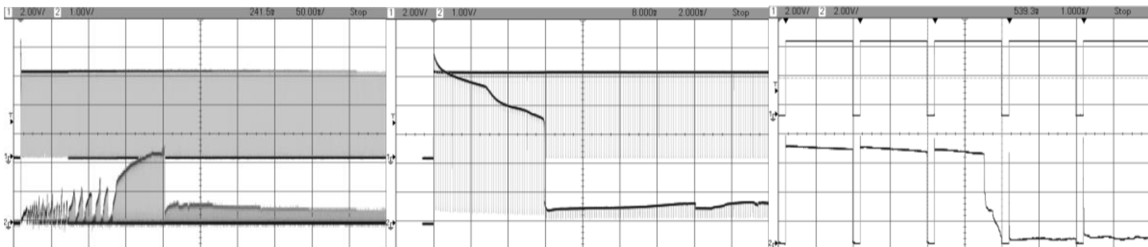


Fig. 4.6: The significant dynamical behavior of the bondwire focused on fusing, pulsed driving sequence (upper trace) and pulsed current through the bondwire (lower trace), selected oscilloscope screenshots (therefore no axis units).

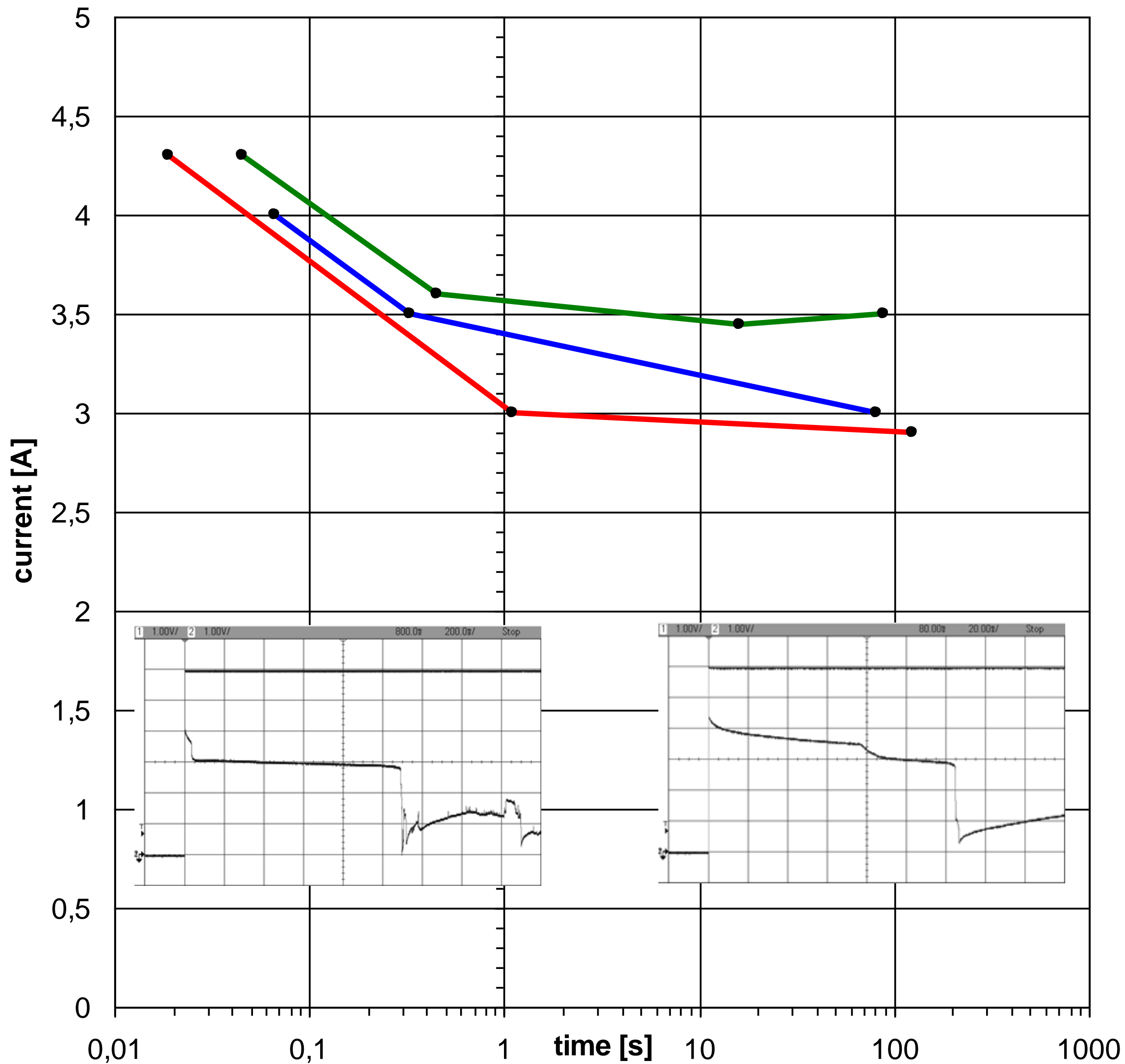


Fig. 4.7: DC bondwire fusing for first (red), sixth (blue) and second (green) Cu 1mil bondwire in a package, oscilloscope screenshots of the voltage drop across the sensing resistor, fusing observed after several seconds.

Test and field data will help the simulation cases. The nanoCOPS initial measurement/calibration tasks will be made by using the AC12050 MMPA chip made by ACCO Semiconductor. This chip contains several PAs for GSM/ EDGE/LTE bands and will be used as an alpha test vehicle for the nanoCOPS measurements. For basic verification of this specific ACCO chip solution the small signal, saturated power and linear power measurements (possible communication bands up to 3 or even 6 GHz) will be provided by BUT.

In parallel of the AC12050 ACCO PA, which is quite complex (different PAs, different technologies) to simulate, smaller dedicated circuits will be used for validation. It will allow to facilitate development and testing of algorithms:

- EM extraction and reduction tests: for validation, different passive structures for probing (inductance, capacitance, balun, lines, resonator,…) have been integrated on different technologies (silicon and BT).
    - For silicon structures, simulations (with the Magwel DevEM tool) will be compared with measurements, with Calibre extraction and Jivaro reduction.
    - For BT structures, simulations (with the Magwel DevEM tool) will be compare with measurements and Momentum (ADS tool from Keysight Technologies) simulations.

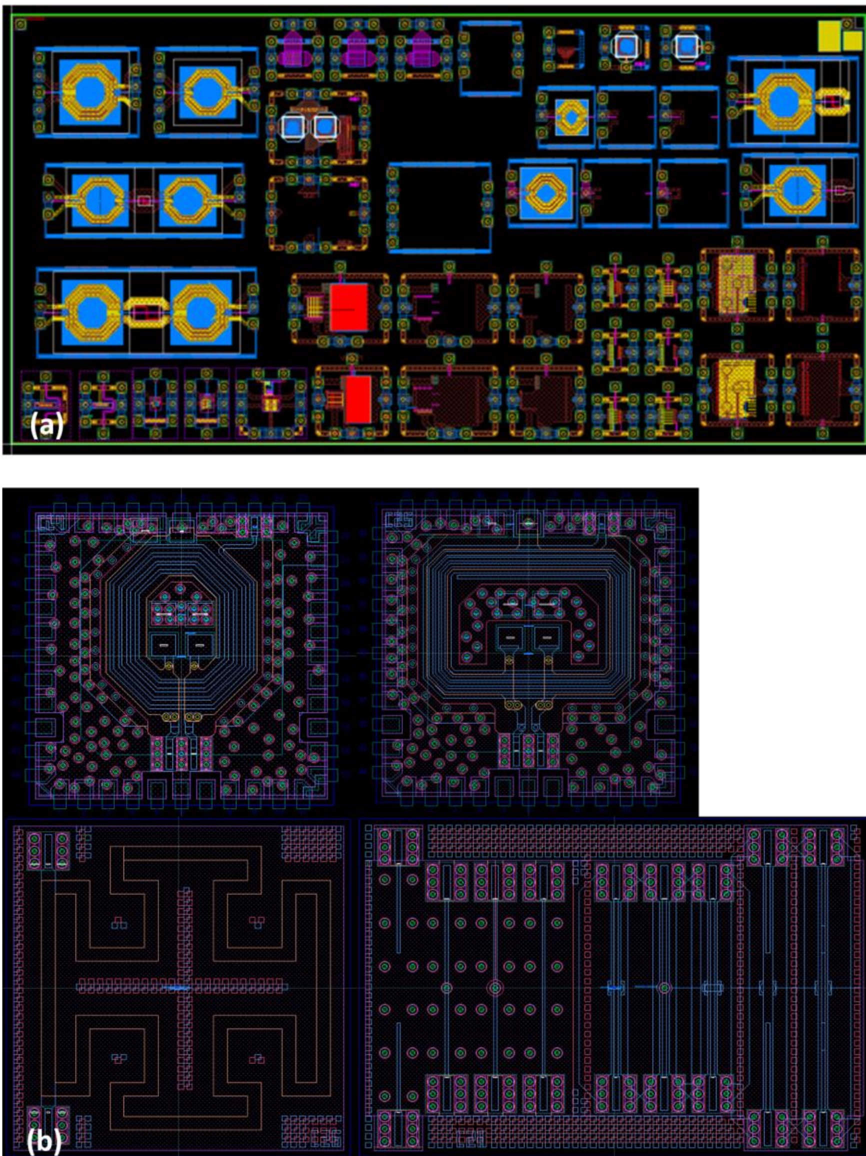


Fig. 4.8: Advanced passive structures on (a) silicon, (b) BT substrate

Measurements were performed in December 2014. In principle, as a validation activity, the focus was on a structure with an inductor and capacitor and comparing this with results from the combined EM simulator (DevEM) and circuit simulator (FHO). Comparison with DevEM (as a standalone tool) will not be part of the validation activities in the nanoCOPS project, since no serious developments will be done on this specific tool itself.

- RF and electro-thermal simulations: A dedicated power stage, designed @ 1.9GHz (band II) in 0.18μm standard CMOS technology will be used for validation. A chip mounted on a PCB delivered 26dBm linear output power (@-40dBc) with 44% efficiency.

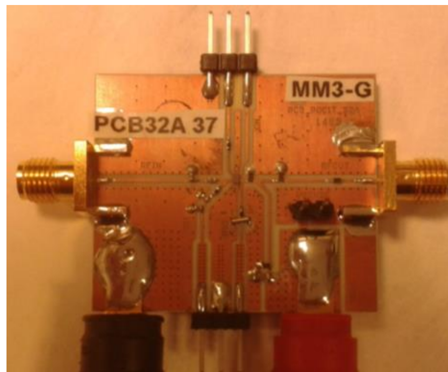


Fig. 4.9: Board testing of the CMOS power stage (Band II, 26dBm linear power)

The first step is to measure temperature dissipation. A test board was prepared with one diode on silicon (to read the transistor junction to ambient thermal resistance Rja) and 2 additional diodes (external) at a different part of the PCB (one on the ground flag and another one on PCB boundary) to measure the PCB dissipation and thermal gradient. Two different measurements have been done:

- For each input power, the diode current was measured (after diode calibration in a thermal chamber) in order to estimate the junction to ambient thermal resistance (Rth_{ja}) and the PCB dissipation (the thermal case to ambient resistance Rth_{ca}).

- To remove the Rth_{ca} inaccuracy, the PCB ground flag temperature was fixed via a cold plate and the junction to case temperature was measured.

RF power measurements were done on a different die and will be compared with electrical simulations (using temperature vs input power measurements) and electro-thermal simulations (Magwel vs Keysight's electro-thermal software) (see also section 3.1).

4.4 *Active tuner approach*

Concerning the PA complex measurement setup, several measurements, such as stability, performance under VSWR, ruggedness, etc., have to be done under termination, where the VSWR for terminating impedance is frequently changed between the ratios 1:3 to 1:10. Passive RF tuners are commonly used for this type of termination.
Modern RF measurement technology is able to replace passive tuners and bring several benefits to this type of tests such as:

- production of intermodulation products (usually produced by passive intermodulation at the antenna stage);
- production of higher power than is produced by the tested PA. So by active tuner technology, the reflected signal from the tuner is greater. Under specified conditions, active tuners are capable to set the working conditions for the output of the PA outside the border of the Smith chart.

Development and implementation of this type of active tuner was the main concern of WP3. This test setup is based on the FlexRIO unit and the RF transceiver module. The basic idea block diagram of active load is given in Fig. 4.10. The active load consists of two parts, the FlexRIO device, which provides the desired signal phase shift and signal attenuation or amplification. The second part is the RF circulator for the incident and reflected wave separation. The directional coupler and vector voltmeter are there for the feedback loop control of the set virtual impedance value (for the control of the VSWR ratio at the output of the PA). Appropriate program control and advanced calibration techniques are needed, but the solution introduces full control over the whole measuring system. Without the feedback loop, there is no control or no information about the VSWR value at the PA output. Full functionality for the continued wave signals is provided. Nowadays we are working towards two directions: first, on the setup for the GSM burst signals and secondly on the replacement of the vector signal voltmeter. In both cases, it is planned to use commonly known USRP radios. This radio is commonly used in the academic sphere and provides good performance. The big issue will be the time synchronization of two units and also their receivers. The USRP could also be used instead of the FlexRIO unit. There will be similar problems with the synchronization of the transceiver and receiver part of the USRP, because the USRP uses two independent PLL based oscillators, which will increase the phase noise and phase measurement uncertainty.

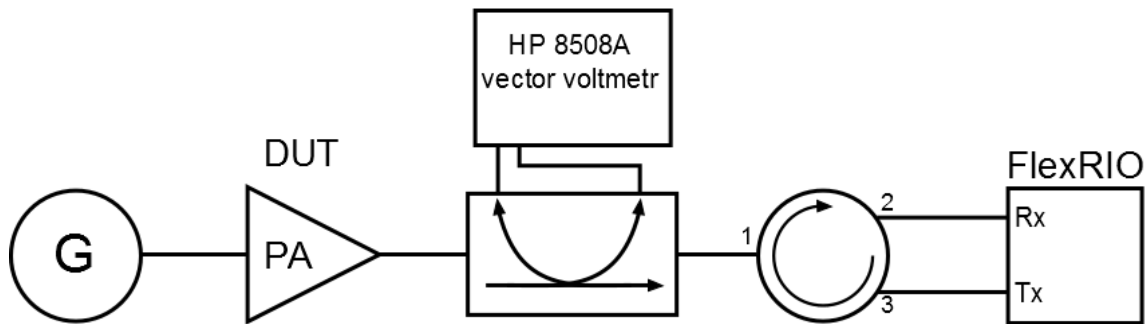


Fig. 4.10: The block diagram of considered active load

For an accurate setup of the terminating impedance, we need to calibrate the vector voltmeter. Calibration requires measurement of short, open and matched impedances at the PA output. This is done by connecting a pre-calibrated VNA instead of the PA and also controlled by the controlling software. The VNA transmits the continuous wave signal to the circulator (port 1) and the FlexRIO generates the reflected wave according to the received signal. The VNA measures the S_{11} and the feedback loop automatically adjusts the value on the VNA to the desired value (short, open and matched load) by changing the parameters of the reflected wave. When the calibration impedance is set, the vector voltmeter provides an amplitude measurement of the incident and reflected waves and also the phase shift. These values are stored for each calibrated impedance and each measuring frequency. According to this stored data, measurement of the PA is corrected and the right impedance for the desired VSWR is set. This setup currently works for the continuous wave signal only.
In the next step we would like to provide a similar system also for the burst signals. There, the old vector voltmeter will be the main limitation, so we are thinking about the usage of the USRP radios in the feedback loop as two synchronized receivers. We also assume that the calibration will be based on similar principles. It means that the calibration will also be done for the continuous wave signals.

4.5 *PA power cell measurements*

Due to the indubitable complexity of the AC12050 MMPA chip made by ACCO Semiconductor, just a single power amplifier (PA) power cell was provided. The cell is denoted as test-board PCB32A-40-1, the operating frequency is 1.9GHz (band II) and the manufacturing process is 0.18µm standard CMOS technology. In order to characterize the PA in the frequency domain and a two-port device, the scattering parameters (S-parameters) will be measured under different ambient temperatures.

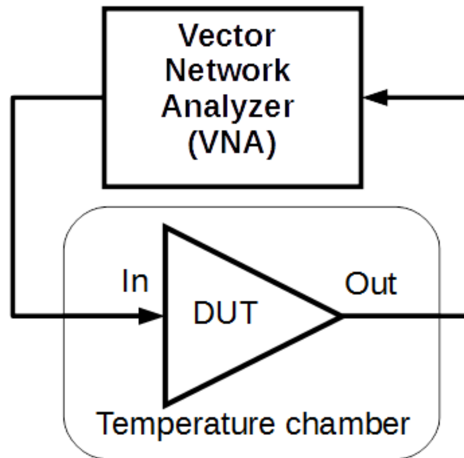


Fig. 4.11: The block diagram of scattering parameter measurement up to 10 GHz.

The block diagram of the proposed measurement test-bench can be seen in Fig. 4.11. The characterization will be done from 9 kHz up to 10 GHz. From the S-parameters the stability factors will be deduced.

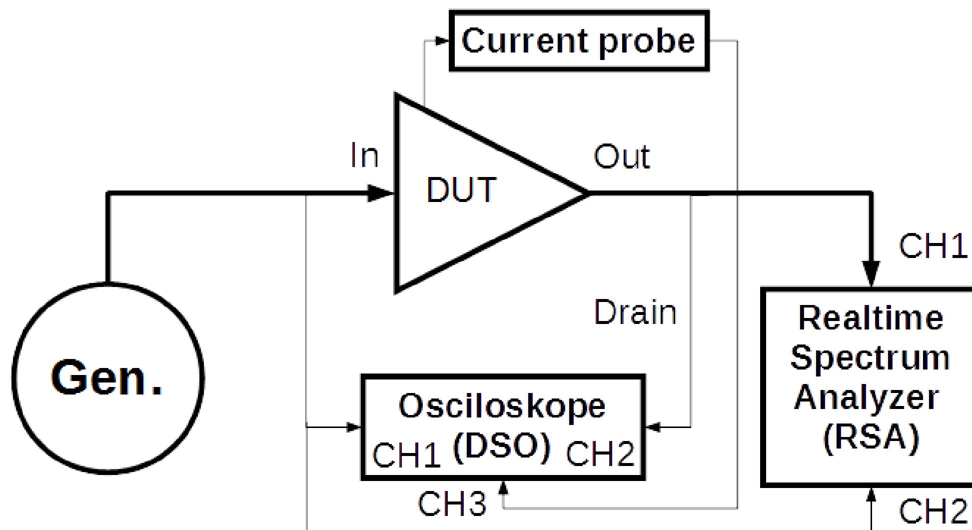


Fig. 4.12: The block diagram of PA characterization.

In order to characterize the PA from the dynamical point of view, modification of the test-bench is necessary. As presented in Fig. 4.12, a signal generator denoted as G is needed. The generator will be configured in order to transmit the WCDMA Rel 99 signal. Parameters, such as input current consumption, output power, gain, Power Added Efficiency (PAE), Adjacent Channel Power Ratio (ACPR), etc., will be measured. The spectral properties will be monitored with a real-time spectrum analyzer. The measurements will be enhanced with an oscilloscope which will be able to monitor the input RF signal and output signal directly on the drain of the amplifier. High-impedance probes are necessary. The

measured results will be compared with simulated results. The proposed test-bench can later be used for AC12050 measurements.

4.6 *Passive components measurements*

Test structures for validation have been integrated for two different technologies. The first set of test structures are on silicon (technology 0.18um with 5 metal layers) and the second set uses BT technology. The contact pad pitch for the provided devices is 200 µm with configuration GSG and GSGSG. For measuring such devices an on-silicon probing technology needs to be used.

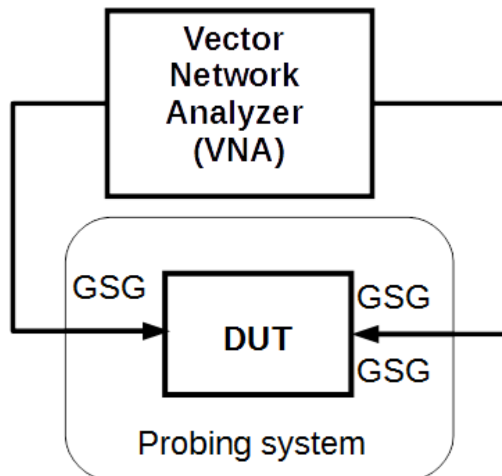


Fig. 4.13: The block diagram of PA characterization.

The layout of the test-bench for EM extraction from silicon and BT devices can be seen in Fig. 4.13. The expected range of measurements is up to 10 GHz. The proposed test-bench is universal enough for measuring general one to three port devices with a pitch of 200 µm.

5 Conclusions

In this deliverable, a clear connection has been made between the development work packages WP1-WP2 and the validation work package WP3. First, validations have been done already making use of available test cases and this work will continue. After that, the link is made between validation of the different tool parts to be developed and the test cases.
In principle, all test cases will be put on the internal website to be used for validation purposes. In addition, a validation plan/document will be kept there as a living document. Whenever validation results become available, they will be put on the internal website as well for verification purposes.
The second part of this deliverable gives a description of the measurement setup, which is the outcome of the first 2 phases of Task 3.3: 1) the design of the measurement methodologies and scenario definitions, based on the partners' requests and inputs regarding expected results in the final stage of the project and 2) after that the realization of the test bed setup and initial measurements, based on current chip solutions of end-user partners.

6 References

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