PROJECT PERIODIC REPORT

Project:	**nanoCOPS - nanoelectronic COupled Problems Solutions**
Project Number:	**FP7-ICT-2013-11/619166**
Work Package:	**WP1 Time-domain Simulation for Coupled Problems**
Deliverable:	**D1.7**
Period covered:	**From 01/10/2013 (M1) to 31/04/2016 (M30)**
Date of preparation:	**19/03/2016**
Date of submission:	**18/05/2016**

Title:	**D1.7 Public Report on pMOR for linear and nonlinear coupled problems.** **Summary: This document is the public report on pMOR for linear and nonlinear coupled problems.**
Partners:	**MPG, TUD, ONN, MAG**
Contact:	**Lihong Feng (MPG)** `{feng}@mpi−magdeburg.mpg.de`
Date:	**May 18, 2016**

D1.7–Public Report on pMOR for linear and nonlinear coupled problems

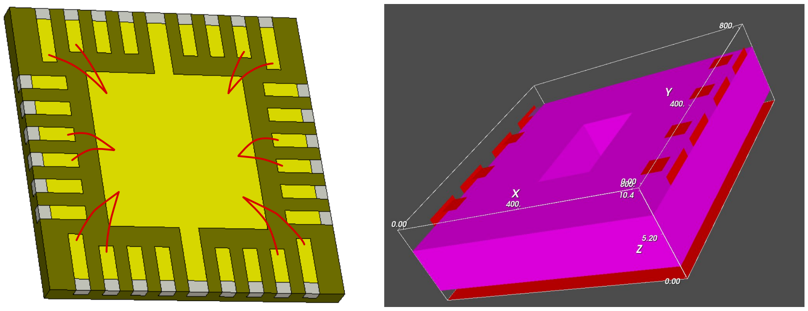
With the scaling down of integrated circuits, thermal issues have attracted increasingly more attention and become a major consideration in design of integrated circuits. Detailed description of electro-thermal problems (see Figure 1) easily leads to very large-scale systems with dimension (degrees of freedom) as high as 10^6, which requires a significant amount of memory in computer simulations. Simulation software, such as Spectre, can often not run the simulation due to memory limitations. Instead, model order reduction [3] computes a reduced-order model (ROM) with much smaller size, which can replace the large-scale system for device- and chip-level simulation, without large-memory requirements. Furthermore, simulation using the ROM can be accomplished much faster than using the detailed system.
In this project, we have developed parametric model order reduction (pMOR) methods [1, 2, 4–8] for ET simulation, especially for being used together with the software ptm-et developed by Magwel NV, and the Cadence circuit simulator Spectre. The accuracy and efficiency of the proposed pMOR methods are validated by both simulation and uncertainty quantification [9] based on reduced-order models (ROMs). In particular,

- the advantages of ptm-et have been inherited by the pMOR methods. As has been described above, ptm-et distinguishes itself from other ET tools by faithfully respecting the intrinsic non-linearity. The pMOR methods developed also preserve the non-linearity present in the ptm-et software. In addition, the ROM-based analysis reproduces the results obtained via ptm-et, with a relative error of approximately less than 10^{-3}, see Table 3. Therefore, the ROM-based analysis is highly accurate and industry-relevant.

- The efficiency of a ROM for a power-cell model of dimension up to 10^7, has been validated in MATLAB, see Table 3. It is very likely that the ROM can be integrated into Spectre to largely accelerate the simulation.

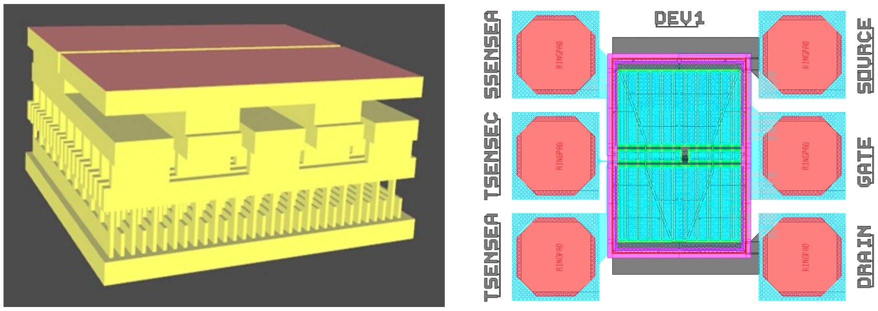
- Compared with physical reduction methods, such as netlist reduction, our pMOR methods achieve a much better reduction in dimension and emphasize more on electro-thermal simulation. For a physical reduction method, it is almost impossible to reproduce the temperature field exactly at all discretized grid points of the full-order model. pMOR, on the contrary, is a projection-based mathematical method, which enables us to only simulate a ROM of very low dimension, and recover the electrical and thermal fields at all grid points. Numerical results show that the developed pMOR methods achieve temperature-field approximation as accurate as electric-field approximation.

- As efficient pMOR methods, moment-matching based methods have received



(a) A microelectronic chip package with applied bond wires.

(b) A package.



(c) A power-MOS device (stretched in the vertical direction).

(d) Layout view of the Power-cell.

Figure 1: Physical models considered in numerical test.

great interest in many fields of applications, among which electronics is arguably the most benefited. However, despite its remarkable efficiency and accuracy, a good error bound has long been an open problem. Therefore, interpolation points and the order of the ROM are selected largely by using experience or even a trial and error approach. For the proposed pMOR method, we have developed an error bond for moment-matching methods, upon which we have constructed an adaptive algorithm, which can automatically select the interpolation points and therefore, automatically build a ROM satisfying a prescribed error tolerance without further specification from users. Numerical results show that the proposed algorithm generates accurate and compact ROMs. Therefore, with a minimal interface and high reliability, the pMOR method proposed is promising for industrial usage.

We use four applications arising from electro-thermal simulations to show the robustness of the derived ROMs: a microelectronic chip package with applied bond wires as shown in Figure 1(a). Here, the interest is to provide simulation tools that are capable of including the very thin bond wires in the simulation to obtain the resulting temperature profile. The second model of a package is shown in Figure 1(b), whose purpose is to allow easy handling and assembly onto printed circuit boards and to protect the devices from damage, and a power-MOS device shown in 1(c), which is commonly used in energy harvesting, where energy from external sources like light and environmental heat are collected in order to power small devices such as implanted biosensors. The fourth application addresses a power-cell model. The power-cell test-case corresponds to a

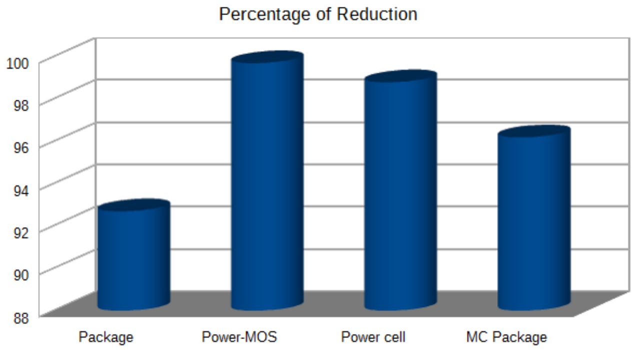
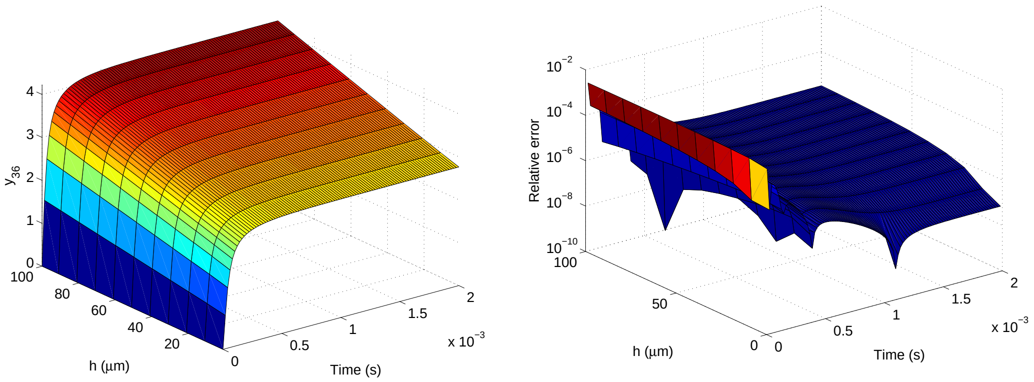


Figure 2: Illustration of reduction percentage in Table 3.

power-transistor design of ONN that is intended for use in smart-power ICs. Besides the core transistor, the cell contains devices allowing to measure the temperature at a central location of the cell as well as devices allowing to obtain a sensing current that is strictly proportional to the total current drain-source of the power-cell. In Figure 1(d), the core transistor layout is surrounded by six bond-pads. Bond-pads on the right are the main terminals of the power transistor, bond-pads on the left are auxiliary terminals for temperature and current sensing. Temperature and current sensors are located in the horizontal row at the middle of the structure. The power transistor is implemented as two main sections located above and below the sensors row.
Table 3 summarizes the information of the ROMs of all models, showing the speedup factor of simulation, and the accuracy of each ROM. It also presents the percentage of size (order) reduction for each model, indicating that each model has been reduced more than 91% in size. In the table, MC package represents the microelectronic chip package model. Figure 2 illustrates the percentage of reduction for the models presented in Table 3.
In Figure 3, we further present the accuracy of the ROM for the package model by plotting the output at port 36, y_{36}, obtained from full simulation of the original large-scale package model (left), and the error of the ROM produced at y_{36} changing with all the parameter samples and time, which shows acceptable accuracy over the whole parameter and time domain. The output of the power-MOS model at the output port

Table 3: Simulation efficiency comparison, n size of the original model, r size of the ROM, l_I number of inputs, l_O number of outputs.

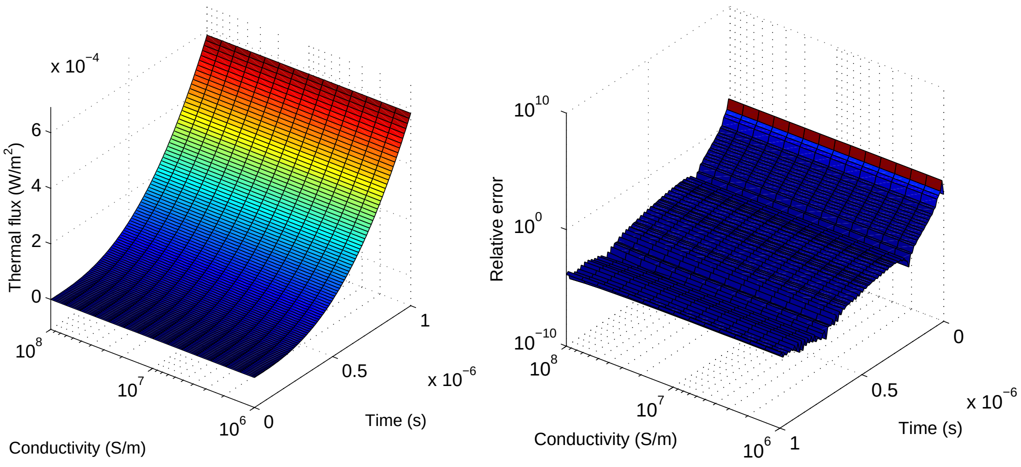
	Original model			ROM			
ET models	n	l_I	l_O	r	Speedup factor	Error	Reduction
MC package	1,323	1	1,323	50	33	1.3×10^{-5}	96.2%
Package	9,193	68	34	673	7.2	3.1×10^{-3}	92.7%
Power-MOS	13,216	6	12	37	65.93	4.1×10^{-4}	99.7%
Power-cell	925,286	408	816	11,245	250	4.0×10^{-4}	99.8%



(a) The thermal flux at port 36, y_{36}.

(b) Relative error at port 36.

Figure 3: The thermal flux and its relative error.



(a) The thermal flux.

(b) The relative error.

Figure 4: The thermal flux and its relative error at the drain.

7, y_7, changing with the parameter and the time, as well as the corresponding relative error of the ROM changing with the parameter and the time are shown in Figure 4. In Figure 4(b), the relative error is large at first because the thermal flux is still very close to zero (the circuit is hardly heated up). As the circuit is heated up, the relative error becomes satisfying. Although the samples are selected within the range $[10^7, 5 \times 10^7]$, the figure shows that the parametric ROM is valid in a much wider range.

References

[1] N. Banagaaya, L. Feng, P. Meuris, W. Schoenmaker, P. Benner: *Model order reduction of an electro-thermal package model.* IFAC-PapersOnLine, 48(1):934-935, 2015.

[2] N. Banagaaya, L. Feng, W. Schoenmaker, P. Meuris, A. Wieers, R. Gillon, P. Benner: *Model Order Reduction for Nanoelectronics Coupled Problems with Many*

Inputs. Proceedings 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE), 313-318, 2016.

[3] P. Benner, S. Gugercin, K. Willcox: *A survey of projection-based model reduction methods for parametric dynamical systems*. SIAM Review, 57(4):483–531, 2015.

[4] P. Benner, L. Feng, W. Schoenmaker, P. Meuris: *nanoCOPS: Parametric Modeling and Model Order Reduction of Coupled Problems.* ECMI Newsletter 56:68-69, 2014. Online.

[5] L. Feng, P. Meuris, W. Schoenmaker, P. Benner: *Parametric and Reduced-Order Modeling for Thermal Analysis of Nanoelectronic Structures*. To appear in Scientific Computing in Electrical Engineering SCEE 2014 (A. Bartel, C. Cimala, M. Clemens, M. Günther, E. Jan W. ter Maten, eds.), series Mathematics in Industry, Springer (2016).

[6] L. Feng, A.C. Antoulas, P. Benner: *Automatic generation of reduced-order models for linear parametric systems*. To appear in Progress in Industrial Mathematics ECMI 2014 (G. Russo, V. Capasso, G. Nicosia, V. Romano, eds.), series Mathematics in Industry, Springer (2016).

[7] L. Feng, A.C. Antoulas and P. Benner: *Some a posteriori error bounds for reduced order modelling of (non-)parametrized linear systems.* Max Planck Institute Magdeburg Preprint MPIMD/15-17, MPI-Magdeburg (October 2015). Available from `http://www.mpi-magdeburg.mpg.de/preprints/`

[8] L. Feng, Y. Yue, N. Banagaaya, P. Meuris, W. Schoenmaker, P. Benner: *Parametric Modeling and Model Order Reduction for (Electro-)Thermal Analysis of Nanoelectronic Structures.* Submitted to Journal Mathematics in Industry (2016).

[9] Y. Yue, L. Feng, P. Meuris, W. Schoenmaker, P. Benner: *Application of Krylov-type Parametric Model Order Reduction in Efficient Uncertainty Quantification of Electro-thermal Circuit Models*. In Proceedings Progress in Electromagnetics Research Symposium, 379–384, 2015.