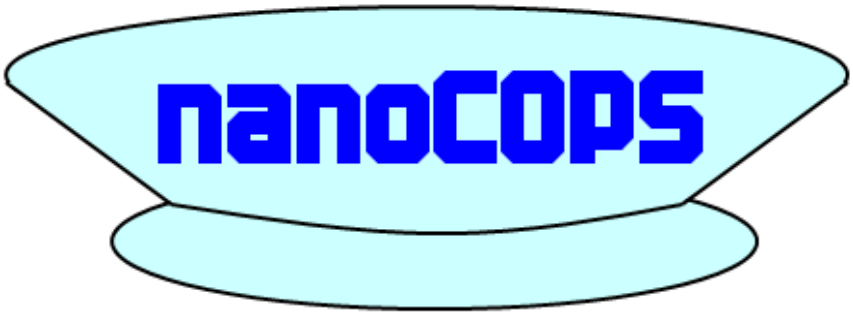

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1 Introduction

The purpose of this document is to serve as a guideline for the actual implementation of the software that is foreseen to be operational at the end of the project runtime.
The nanoCOPS project addresses the simulation of two technically and commercially important problem classes identified by our industrial partners ("Use Cases"):

- **Power-MOS devices**, with applications in energy harvesting, that involve couplings between electromagnetics (EM), heat, and stress, and
- **RF-circuitry** in wireless communication, which involves EM-circuit-heat coupling and multirate behaviour, together with analogue-digital signals.

The scientific challenges are to create efficient and robust simulation techniques for strongly coupled systems, that exploit the different dynamics of sub-systems and that allow designers to predict reliability and ageing.
This document will emphasize on the coupled problem of electro-thermal simulation. In particular, fully coupled simulation and co-simulation will be considered.

2 Use Cases

With the increased need of smart grids for a sustainable energy infrastructure, **power devices** play an important role in, both, energy harvesting and distribution and thus in controlling overall energy efficiency. Automotive applications are also an important field that requires the handling of demanding electro-thermal operational constraints to the design of both components and systems. Power devices consist of several thousands of parallel channel devices to deliver high throughput of current and/or current control in both CMOS and bipolar technology. The layout of metal interconnects, bond pads, and bondwires (or bumps/balls) of large-area power semiconductor devices has a profound effect on metal de-biasing, device ON-resistance (Rdson, or RDS(on)[1]) and reliability (electro-migration, thermal-induced stress, device & material life times, etc.). Metal-interconnects resistance is especially critical in the context of large-area devices that are designed to have a very low (up to a few tens of milliohms) Rdson value [6].

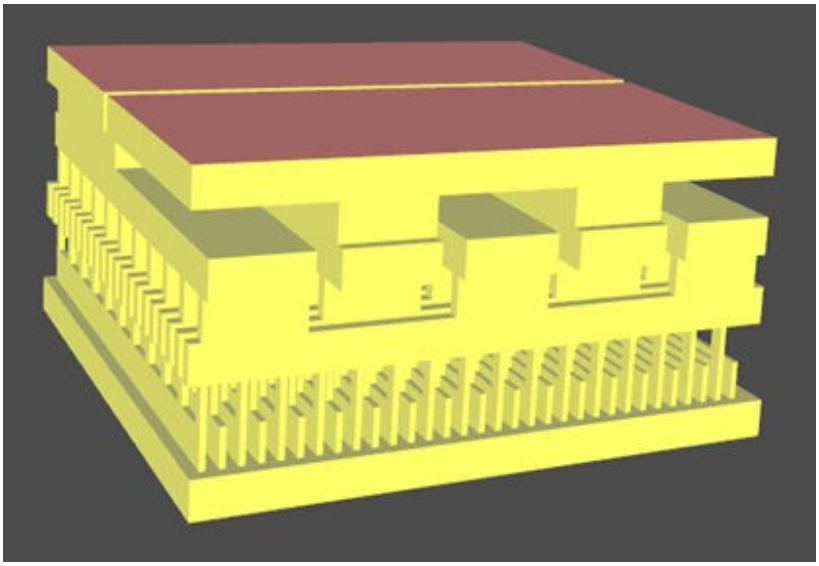

Figure 1. Typical layout of the power transistor (stretched vertical direction) showing its complex geometry.

[1] RDS(on)=V_{ds}/I_{ds}

In order to get a glance of a power device, Use Case 1, Fig. 1 shows the complex geometrical finger structure in a typical device design of a **power transistor,** using six layers of metal. The source drain contacts are located at the top of the design. A series of metal stripes and via patterns will ultimately transport the current to the drains and away from the sources of the individual channels. Having found the electro-thermal solution, hot spot detectors (design-rule checking) can be activated to post-check the full power transistor array. The current flow is really multi-dimensional.

For being able to model and simulate such devices we first need to accurately capture the complicated current-flow patterns in such devices with complicated top metal layouts constrained by the package, wire bonding, or ball array requirements. The design challenge is further increased by the need to separate out the consequences of the **competing physical effects**, which are **strongly coupled**, and moreover depend on the time-dependent input stimuli.

Several approaches for electro-thermal simulations of power DMOS transistors have been presented, e.g,. [3,4,7,9,10,13,17,19,22,24]. In most approaches, the DMOS is divided into several parts to account for nonuniform temperatures and different power densities. Different thermal simulator strategies are proposed, e.g., in [4,10,17,19,24], the thermal characteristics of an integrated circuit is analyzed by discretizing the layout information in a layered fashion. The thermal equations are solved on the generated mesh. This analysis method starts from an electrically characterized structure: electrical power dissipation is known on beforehand and used as an input parameter in the simulation.

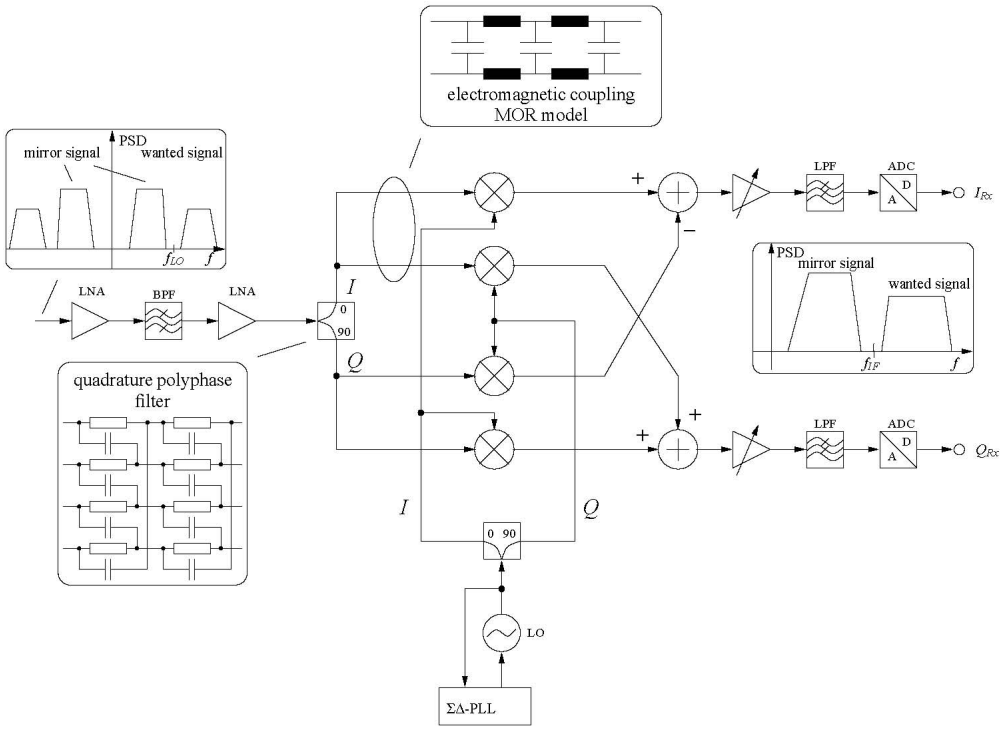

Figure 2. Block diagram of a low-IF or zero-IF receiver architecture with an image reject filter and a quadrature mixer stage.

The second use case is depicted in Fig. 2: the schematic shows the building blocks of a receiver chain including LNAs, mixer stage, quadrature splitters, VGAs, and filters. The image rejection of the inphase and quadrature phase I/Q depends critically on the device variations due to the fabrication process which is addressed by Uncertainty Quantification (UQ). Especially critical are the mixers and the quadrature filters. Due to self-heating the image rejection may be diluted during operation.

3 Simulation Techniques

Co-simulation for electromagnetic-heat coupling [2,20] has industrially been used in [11,16]. Even changes due to exceeding the Curie temperature could be dealt with. In [12] the technique was improved by further iteration and one did prove convergence under mild conditions. In [5,8,14,23] strong couplings did prefer for a fully coupled solution approach.
In this co-simulation approach the electrical and thermal problems are solved sequentially and are loosely coupled. When needed, iterations are performed across both solvers to find a converged solution using a waveform relaxation technique, e.g. [2,12]. These approaches are commonly very efficient if the switching frequencies in the circuit or in the electromagnetic field are much higher than the changes in the thermal field. However, if the time constants in all systems are similar, then waveform relaxation tends to be much slower than a direct solution using Newton-Raphson techniques. In neither case convergence is guaranteed but can be verified by analyzing the problem structure and large classes of problems are known to work. The analysis is similar to the case of classical iterative methods for linear systems where the eigenvalues of the systems have to be inspected. One also has to distinguish between time-domain simulation and steady-state analysis.
In other approaches, equivalent thermal networks are extracted from a temperature simulator and used in circuit simulation [6]. As an alternative approach, in [7,13,22] two coupled net lists are generated of the structure: an electrical net list and a thermal net list, which are then solved in a standard circuit simulator.
Co-simulation with a circuit simulator was also suggested [1,3,9,20,21]. Similar remarks apply to this situation.

All approaches described above require a careful bookkeeping of the interaction between electrical and thermal variables. Iterative approaches complicate the software architecture and its maintenance due to the iteration loop and the additional bookkeeping. On the other hand they allow for easier parallelization and encapsulate solvers in an objective-oriented programming fashion.

To avoid the disadvantages of weak coupling, the implementation at Magwel deals with the electro-thermal problem in an ab-initio self-consistent manner. Electrical and thermal equations are solved simultaneously and self-consistently from a single set of equations as opposed to decoupled solutions commonly used in other approaches. A high spatial resolution allows accurate modeling of metal layers as required for advanced integrated BCD technologies. At the same time, the simulator uses a well-adapted mesh for the substrate, which is important for the simulation of the temperature. Thus, both the voltage drop in the on-chip metallization as well as the device temperatures can be determined without sacrificing accuracy or limiting the applicability of the simulator to special cases. Joule self-heating and heat flow in metal is modeled together with non-linear temperature dependent electrical and thermal resistivity's and thermal capacitances of materials. The electrical and thermal behavior of active area transistors is modeled with non-linear table models. The generated Joule heat is considered not only for MOS and Bipolar devices, but also for interconnects. A fixed or variable temperature, a time dependent heat flow, and adiabatic or convective boundary conditions can be applied through contacts (rectangular shapes which can be placed anywhere in or around the device or the die), together

with modelling the thermal resistance of bond wires. Further, die, die-attach, mold compound, lead-frame, leads and other elements in the thermal path are modeled with package models, which are readily imported from a package data base.

4 Dynamic Electro-thermal nonlinear model

The metallization stack is a multi-layered structure consisting of dielectric, vias, contacts, and metal interconnect structures which are meshed in 3D. Actually, although electrical and thermal models are in essence described by linear (Poisson) models, non-linear elements enter the simulation in two ways:

1. Joule self-heating and heat flow in metal.
2. Electrical and thermal conductivities of both metal and substrate are temperature dependent. This is necessary for accurate simulations of large temperature swings for instance in failure conditions like short circuits as well as non-linear temperature dependent electrical and thermal resistivities.

Although both mechanisms are important we will ignore the nonlinear material properties for the time being.

The thermal boundary conditions are modeled by thermal contacts (2D rectangular shapes), which can be placed anywhere on the surface of the die or anywhere inside the chip. Thermal contacts have a constant temperature over the surface of the contact. A fixed or time variable temperature can be applied directly to the contact, or indirectly through a thermal resistance that is attached to the contact. A back contact under the die can, for example, be put at the room temperature to model a heat sink. Die-attach, mold, lead-frame, leads and other elements in the thermal path can be modeled with 3D structures. The bond wires are modeled as discrete elements with a thermal resistance. The heat Q_{out} removed from the device is an area integral over the thermal contacts:

$$Q_{out}(t) = \int \kappa \cdot \nabla T \cdot dS, \qquad (1)$$

where κ is the thermal conductivity and T the temperature, respectively. Thermal contacts can also be used as fixed or variable (time-dependent) 2D heat generators or cooling elements, which provide a uniform heat flux (positive or negative) through its surface but where the temperature distribution over the contact surface needs not to be uniform.

Electric field solver aspects

The electrical part of the integrated field solver [15,18] addresses the current-continuity equation:

$$\nabla \cdot J + \frac{\partial \rho}{\partial t} = 0 \,,\; J = \sigma \cdot E \,,\; E = -\nabla V \qquad (2)$$
$$\rho = -\nabla \cdot (\epsilon \nabla V)$$

where J is the current density, E the electrical field, V the electrical potential, σ the electrical conductivity, ε the permittivity, and ρ the charge density. Since we do not consider local charging effects, i.e. ρ=0, the current-continuity equation (2) reduces to a Poisson problem for conductive domains, being interconnects and active devices. The power dissipation is located mainly in the

active material constituting the transistor fingers, and to a lesser degree in the interconnect metallization.

Thermal field solver aspects

The thermal part of the solver addresses the heat equation

$$\begin{aligned} \nabla \cdot \Phi_q + \frac{\partial w(T)}{\partial t} &= \mathrm{Q} \\ \Phi_q &= -\kappa \nabla T \\ w(T) &= C_T\left(T - T_{ref}\right) \end{aligned} \qquad (3)$$

Here, $\mathbf{\Phi_q}$ is the heat flux and w the local energy storage, characterized by the thermal capacitance C_T. Q represents heat sources or sinks.
The solution of this equation provides the desired temperature information to feed into (2). However, the solution is only computable, provided that the heat source is known. The source may consist of several contributors. The boundaries of the simulation domain may contain heat-injecting or extracting properties. Besides these sources, the Joule self-heating is of particular interest:

$$Q_{SH} = E \cdot J \qquad (4)$$

Note that this nonlinear term is determined by (2), and therefore it is mandatory to solve (2) and (3) simultaneously.
The side walls of the simulation domain are dealt with using Neumann (= adiabatic) boundary conditions. This corresponds to ideal, thermally and electrically insulating walls, which is a valid assumption for the applications considered here.

State space description

After meshing the domain we solve the set of equations (1-4). This gives rise to a matrix of size 2N x 2N, where the system contains N electrical and N thermal degrees of freedom (DOF). The energy is transferred through the border of the simulation domain through M ports. The boundary conditions at these ports are defined for either voltage or current and temperature or thermal flux. The state space of such a system becomes:

$$E\frac{\partial x}{\partial t} = A \cdot x + B \cdot u \qquad (5)$$

$$y = C \cdot x + D \cdot u \qquad (6)$$

Here x denotes the state space variables (2N), where u and y describe the input (N_i) and output (N_o), resp. Therefore the state space matrices have the following dimensions: A(2Nx2N), B(2NxN_i), C(N_ox2N), D(N_oxN_i) and E(2Nx2N), and the input and output vectors look like: u(N_i) and y(N_o).
It is clear that this only describes the linear part of the system, and non-linear elements must be brought in separately. The self-heating Q_{SH} described in (4) is a non-linear source term in (3). It is

part of the thermal equation and proportional to the square of the voltage difference. This will give rise to two new tensors in (5). The nonlinear contributions are covered by the tensor F in (7), which gives the coupling of the Joule heating to the thermal DOF's, and the tensor G, which describes the Joule heating connection to the input variables u.

$$E\frac{\partial x}{\partial t} = A \cdot x + B \cdot u + F \cdot xx + G \cdot xu \qquad (7)$$

The dimensions of F are (2Nx2Nx2N), while G's dimensions are given by ($2Nx2NxN_i$). Although both tensors need to be calculated, the influence of G on the model is quite limited, and for the time being we can ignore it.

Static example for test purposes

A first test case is shown in Fig. 2.

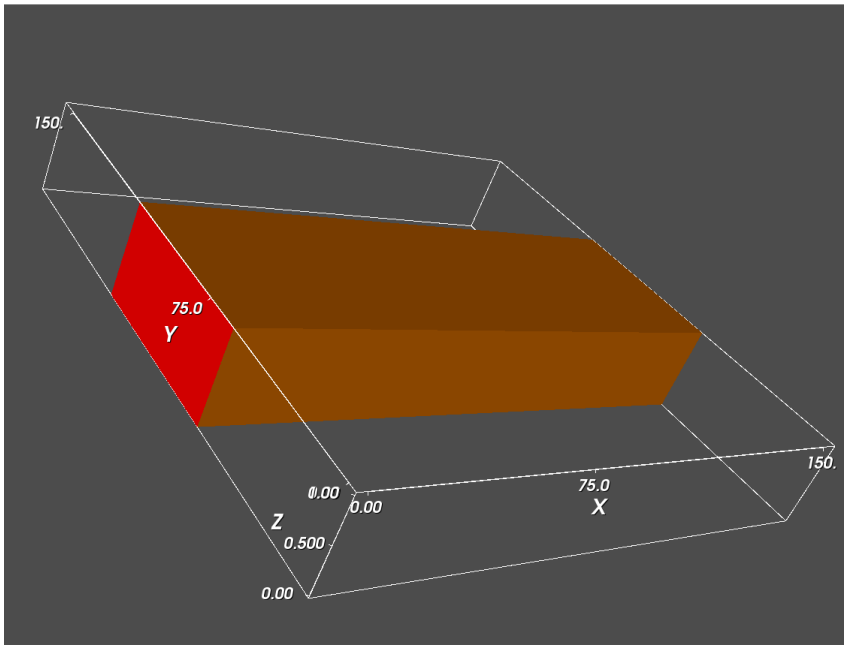

Figure 2. A simple metal line, with two contacts. The dimension of the metal is 50µm x 150µm x 1µm. As electric boundary conditions, we apply 10V and 0V on the contacts. Thermally, the contacts are kept at a fixed temperature of 0 °C.

When an electrical current flows through the metal wire, Joule heat will be dissipated, and a parabolic temperature distribution is build inside the wire (see Fig. 3).

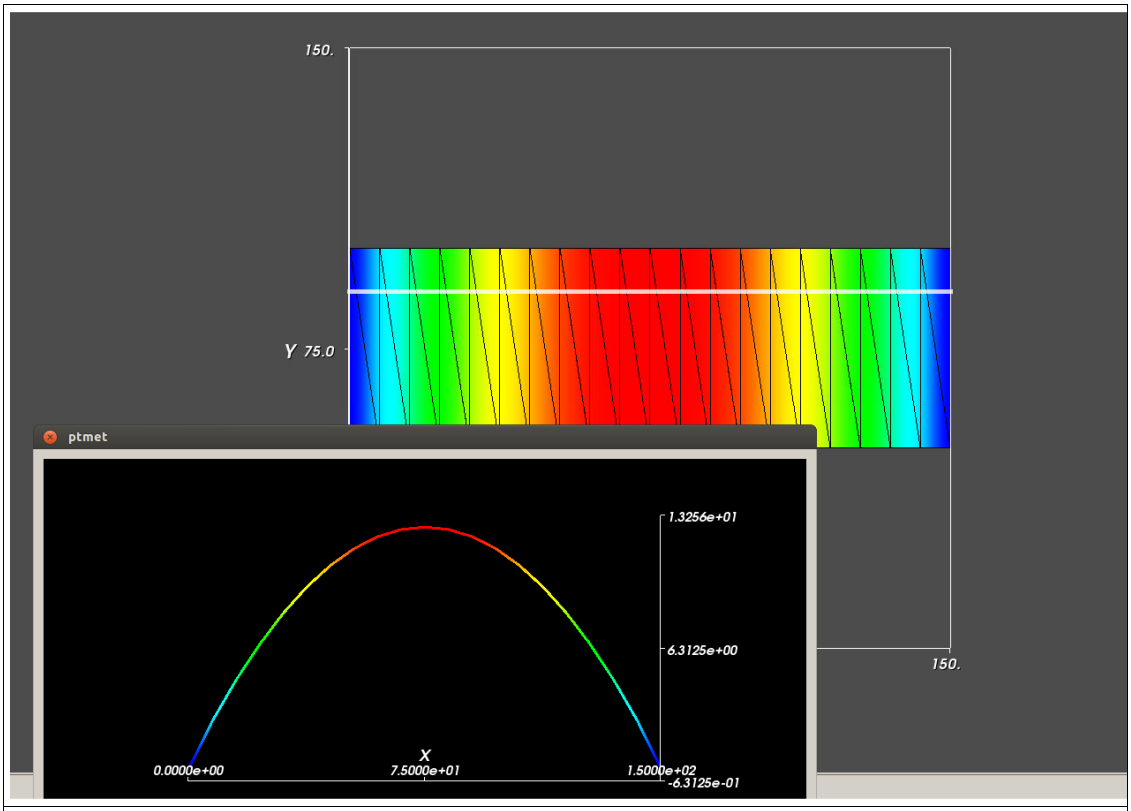

Figure 3. The quadratic temperature distribution inside the wire for a voltage difference of 10V, and a current of 33.3A. The conductivity of the metal is taken to be 1.0e7S/m and the thermal conductivity is 1.0e7W/mK.

The state space matrices A, B, C, D, F are computed for a mesh with 10 mesh volumes along the wire. Note that we do not take into account the E matrix as the example is still static. Also the influence of the G tensor is neglected, which is valid provided that the mesh is sufficiently dense. These state space matrices are used as an input for a Newton-Raphson scheme, solving the system (6-7).
This Newton-Raphson scheme produces for an input vector

V1 = 10 [V]
V2 = 0 [V]
T1 = 0 [°C]
T2 = 0 [°C]

the following output vector:

I1= -33.33333 [A]
I2= 33.33333 [A]
V1 = 10.00000 [V]
V2 = 0.00000 [V]
Flux1 = 150.00000 [W/m2]
Flux2 = 150.00000 [W/m2]
T1= 0.00000 [°C]
T2= 0.00000 [°C]

In order to get used to the examples, we add three versions of this test case:

name	mesh nodes	N	Ni	No
TCTYA	84	76	4	8
TCTYB	164	156	4	8
TCTYC	1620	340	4	8

5 Design of the software for electro-thermal co-simulation

As is illustrated by the example above, several software components are needed to achieve the co-simulation. The core ingredient is an electro-thermal *holistic* solver. This solver (provided by MAG) addressed the electrical equation (2) and the temperature equation (3) in a simultaneous way. Currently, both equations are discretized on a single mesh, boundary conditions are inserted and the electro-thermal transport is computed using a simultaneous solver for the Newton-Raphson non-linear solver. Of course this is an expensive process in the case when the simulation domain becomes large and requires many mesh nodes to cover it fairly accurately for capturing thermal gradients. Therefore, it is desired to exploit reduced-order modeling methods to replace parts of the simulation domain by compact models, which can also be reduced state-space models. The reduced or compact models interact with the field solver via the specifically designed boundary conditions. The latter are realized by identifying two-dimensional tiles which are seen as contact location by the field solver and as I/O variables by the ROM tools. The benefit of the reduction is felt in two ways: (1) The number of degrees of freedom gets reduced because some regions of the simulation domain are excluded, (2) the mesh generator does not need to introduce nodes in the non-excluded region, which were otherwise generated as a side effect of meshing of the excluded domains.
A communication bridge needs to be established between the ET field solver and the ROM solver.
Anticipating the final project goals, the combined solver should finally produce models that are readable by third party tools, such as Spectre, in order to have the results of the simulations seamlessly integrated in the design process (flow). At the front-end, e.g. before launch of the simulation, the design-flow integration must also be respected. It means that the field solver is capable of reading and process layout data and technology data. The layout data is available in a gds file and the technology data is found in the itf (interconnect-technology file).

Bringing together above criteria, we arrive at the software design depicted in Fig. 4.

6 Conclusion

This document describes a high-level software design for the electro-thermal simulation tool. We did not present here the details concerning concrete realizations of the data storage, flows and algorithms concerning discretization. These technical details are strongly connected to the selection of software design tools, languages and rather standard Finite-Integration techniques. However, we have presented the coherence of the various contributions leading to a fully integrated simulation tool.
The implications for co-simulation on the software will be discussed further at the 2nd nanoCOPS Workshop at HUB in Berlin, on Oct. 6/7, 2014.

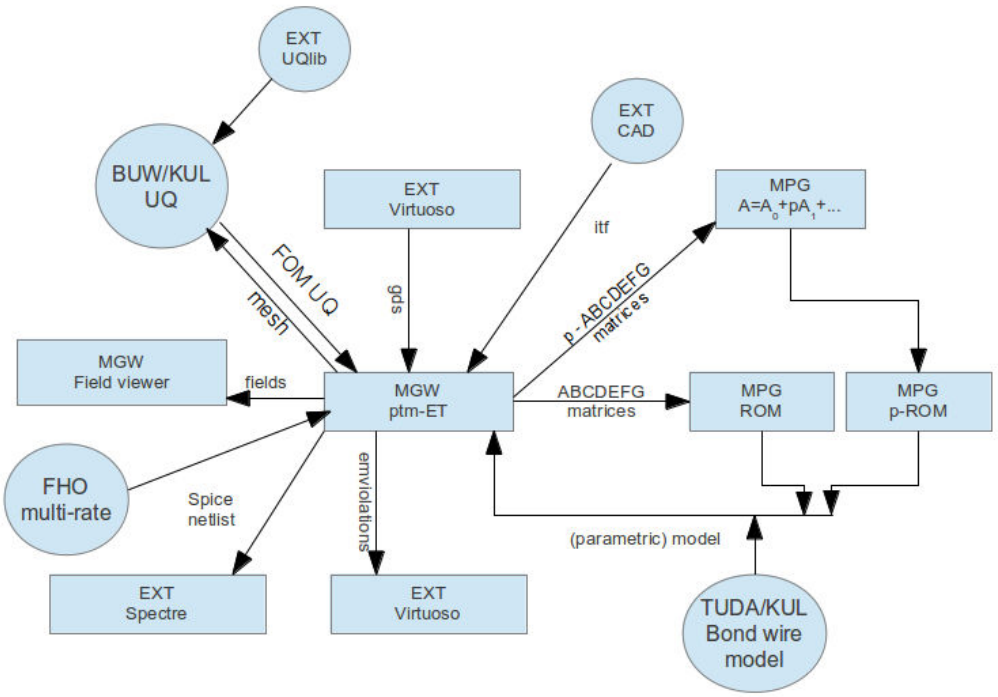

Figure 4. Software Design Scheme. The nanoCOPS module providers are denoted as MGW, MPG, TUDA/KUL and BUW. External software modules are denoted by EXT. Arrows represent data flows.

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